Daisy Board User Guide

Revision 1.1

2019. 12. 30

CRZ Technology

http://www.mangoboard.com/

Document History

Revision	Date	Change note
1.0	2019.10.01	First draft
1.1	2019.12.30	First Release

Table of Contents

1. Overivew

1.1. Block Diagram

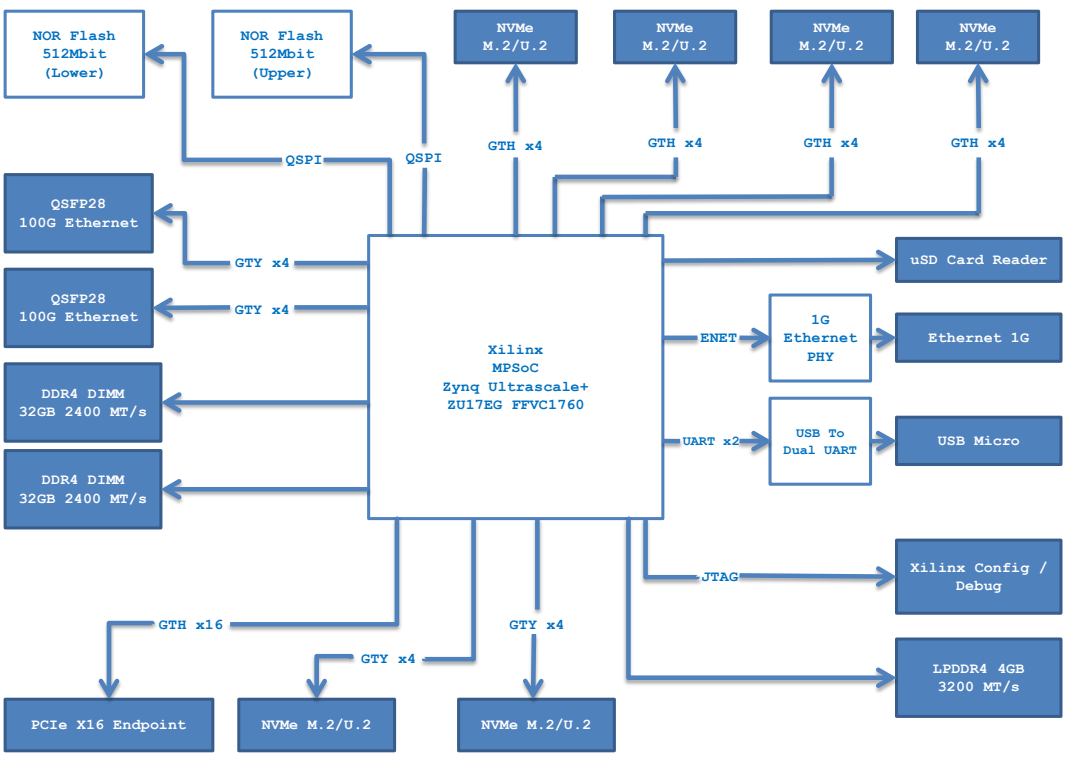
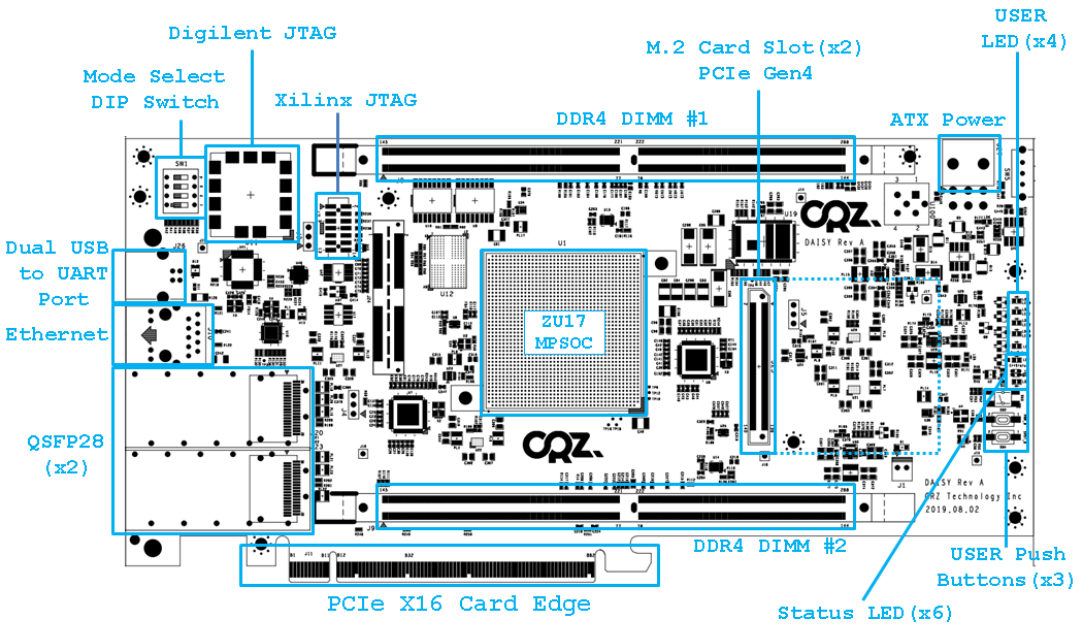


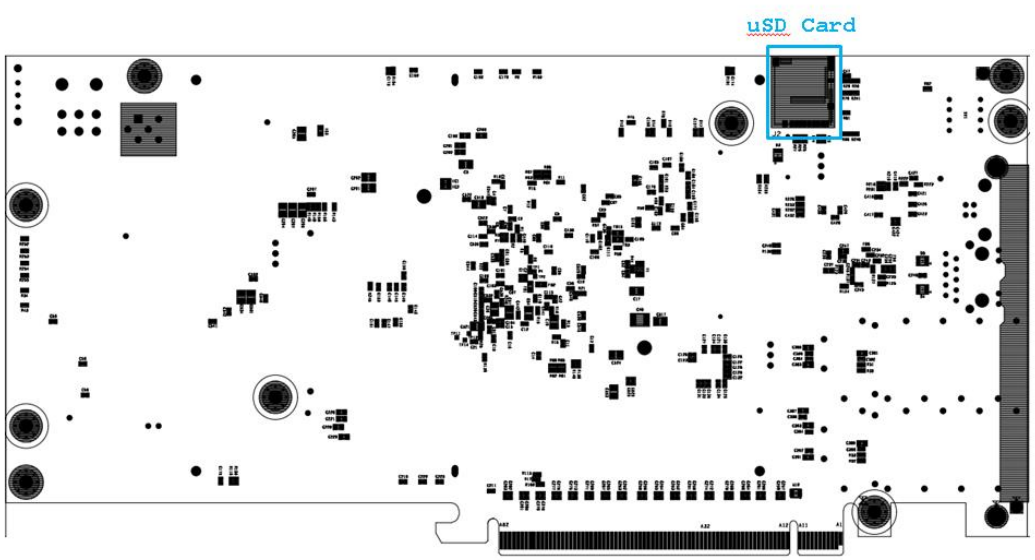
Figure 1. High Level Block Diagram

1.2. Board Layout



Front/Top(primary) side of Board

Figure 2. Daisy Physical Layout: Front, Top



Back/Bottom(secondary) side of Board

Figure 3. Daisy Physical Layout: Back, Bottom

2. LEDs and Connectors

2.1. Status LED

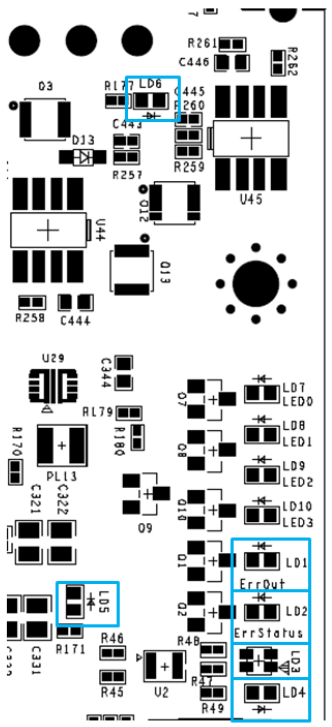


Figure 4. Status LED

Color	Board Label	Pin Name	Pin	Device
GREEN/RED	LD3	PS_INIT_B	V27	**U1**
GREEN	LD4	PS_DONE	Y28	
RED	ErrOut(LD1)	PS_ERR_OUT	U27	
RED	ErrStatus(LD2)	PS_ERR_STATUS	V28	

Table 1. MPSOC Status LED

Color	Board Label	Description
GREEN	LD5	3V3 rail power good signal
GREEN	LD6	12V available from J27 ATX connector or J11 PCIE Host

Table 2. Power Status LED

2.2. User LEDs

There are 4 LEDs connected to PL part. All these LEDs are active High. Please refer to the following Figure and table.

- High on output = LED is ON
- Low or Tri-state = LED is OFF

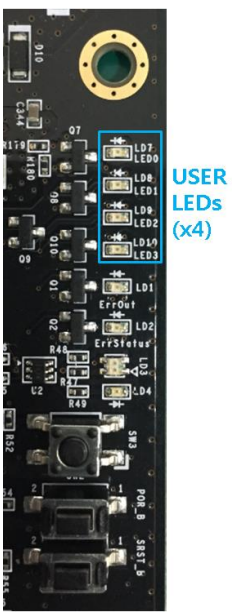


Figure 5. PL-GPIO LEDs

Color	Board Label	MPSOC		Description
		Pin Name	Pin	
RED	LED0(LD7)	B94_IO/L4_P/AD12_P	E1	User LED
RED	LED1(LD8)	B94_IO/L4_N/AD12_N	D1	User LED
RED	LED2(LD9)	B94_IO/L3_P/AD13_P	E3	User LED
RED	LED3(LD10)	B94_IO/L3_N/AD13_N	E2	User LED

Table 3. User LEDs

2.3. JTAG Connector Pinout[J7]

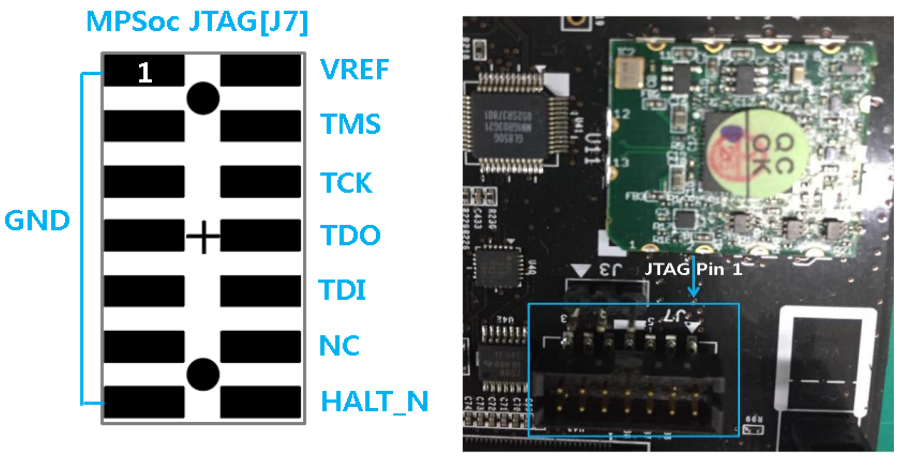


Figure 6. JTAG Connector[J7]

Device	Pin	Pin Name	Schematic Net Name	Pin	Device
			VCC_3V3	2	J7
U1	AD26	B503_PS_JTAG_TMS	JTAG_TMS	4	
	AC26	B503_PS_JTAG_TCK	JTAG_TCK	6	
	AD27	B503_PS_JTAG_TDO	JTAG_TDO	8	
	AD25	B503_PS_JTAG_TDI	JTAG_TDI	10	
			NO CONNECT	12	
U34	3	2A	PS_ARM_JTAG_SRST_B	14	
			GND	1	
				3	
				5	
				7	
				9	
				11	
				13	

Table 4. Xilinx Config/Debug[J7] 신호 연결

2.4. uSD Card Reader[J2]

Schematic Net Name	MPSOC		Device
	Pin Name	Pin	
SDIO_DETECT	B501_PS_MIO45	T29	U1
SDIO_D0	B501_PS_MIO46	U28	
SDIO_D1	B501_PS_MIO47	T28	
SDIO_D2	B501_PS_MIO48	V30	
SDIO_D3	B501_PS_MIO49	U29	
SDIO_CMD	B501_PS_MIO50	V29	
SDIO_CLK	B501_PS_MIO51	W30	

Table 5. uSD Card Reader[J2] 신호 연결

2.5. 2 Pin Fan connector[J1]

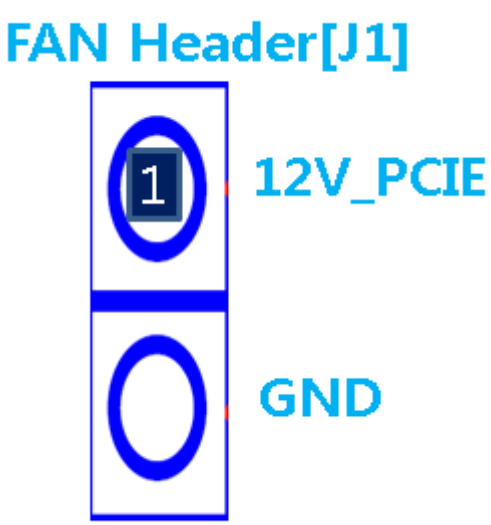
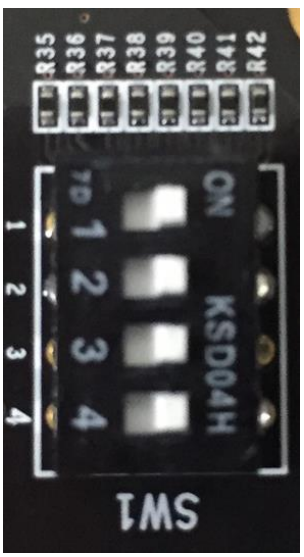


Figure 7. DC Fan Breakout Header

3. Operation Information

3.1. Mode Select DIP Switch [SW1]

There is DIP switch to select Boot mode.



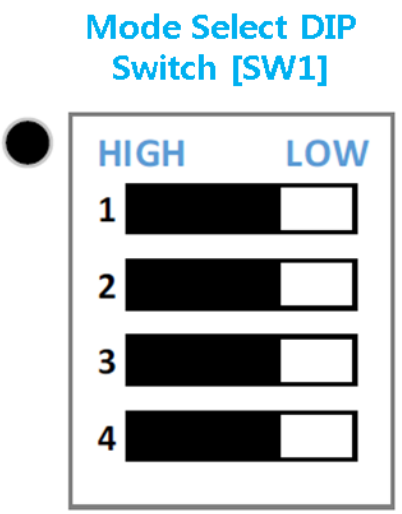


Figure 8. Mode select DIP switch

MODE	Switch			
	[4]	[3]	[2]	[1]
JTAG	LOW	LOW	LOW	LOW
QSPI 32	LOW	LOW	HIGH	LOW
SD1	HIGH	HIGH	HIGH	LOW

Table 6. Mode select table

Switch	MPSOC	
	Pin Name	Pin
1	B503_PS_MODE0	AA27
2	B503_PS_MODE1	AC28
3	B503_PS_MODE2	AA28
4	B503_PS_MODE3	AB28

Table 7. Pin assignment for Mode select DIP switch

3.2. PUSH buttons

There are 3 push buttons and the default value is high.

- Button released = HIGH
- Button pressed = LOW

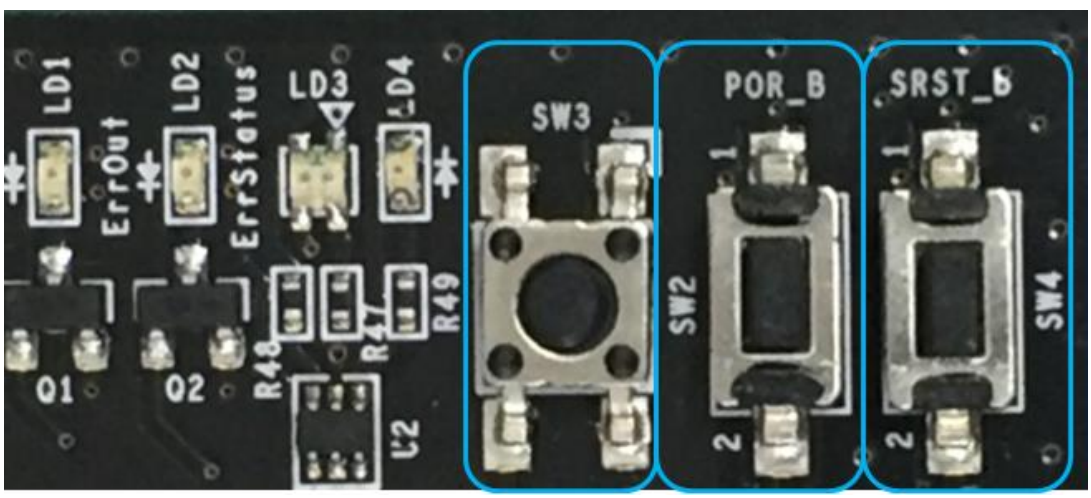


Figure 9. Push buttons

Device	Board Label	MPSOC	
		Pin Name	Pin
SW2	POR_B	B503_PS_POR_B	W27
SW3	SW3	B503_PS_PROG_B	Y27
SW4	SRST_B	B503_PS_SRST_B	AB27

Table 8. Signal assignment of push buttons

3.3. I2C bus interfaces

There are multiple I2C buses to communicate with several other devices. The block diagram below shows all I2C connections on the board.

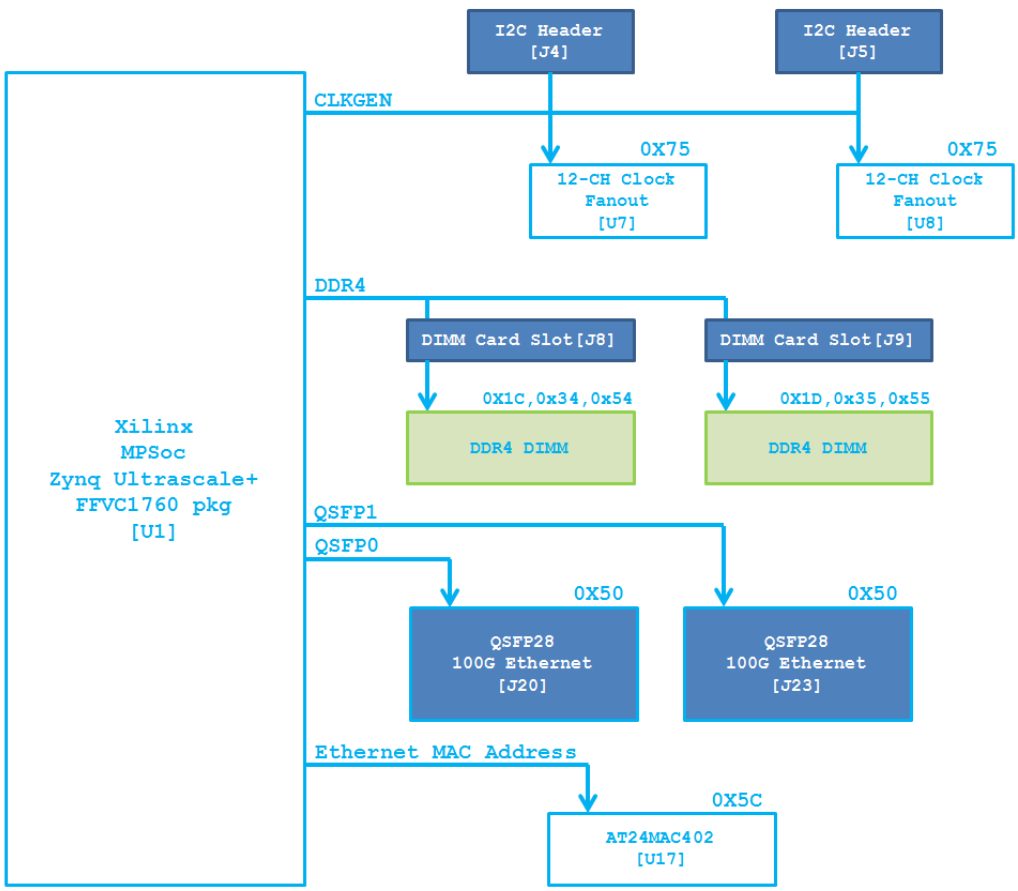


Figure 10. I2C Bus Block Diagram

The "CLKGEN" I2C bus is can be accessed via a 3-pin header(J4, J5)

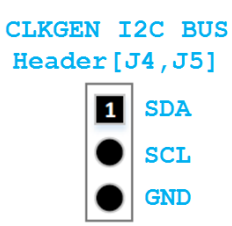


Figure 11. CLKGEN I2C Bus Header

Device	Bus Name	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	CLKGEN	AJ32	B500_PS_MIO14	SI5391_0_SCL	SCLK	16	U7
		AD35	B500_PS_MIO15	SI5391_0_SDA	SDA/SDIO	18	
		AJ31	B500_PS_MIO16	SI5391_1_SCL	SCLK	16	U8
		AJ30	B500_PS_MIO17	SI5391_1_SDA	SDA/SDIO	18	
	Ethernet MAC	AJ31	B500_PS_MIO16	PS_I2C1_SCL	SCL	6	U17
		AJ30	B500_PS_MIO17	PS_I2C1_SDA	SDA	5	
	DDR4	AJ32	B500_PS_MIO14	PS_I2C0_SCL	SCL	141	J8
					SCL	141	J9
		AD35	B500_PS_MIO15	PS_I2C0_SDA	SDA	285	J8
					SDA	285	J9
	QSFP0	AJ32	B500_PS_MIO14	PS_I2C0_SCL	SCL	11	J20
		AD35	B500_PS_MIO15	PS_I2C0_SDA	SDA	12	
	QSFP1	AJ31	B500_PS_MIO16	PS_I2C1_SCL	SCL	11	J23
		AJ30	B500_PS_MIO17	PS_I2C1_SDA	SDA	12	

Table 9. Pin assignment of I2C Bus

4. Loopback board

There is loopback board helpful for development and testing

- NVME M.2 Loopback Card

4.1. NVME M.2 Loopback Card

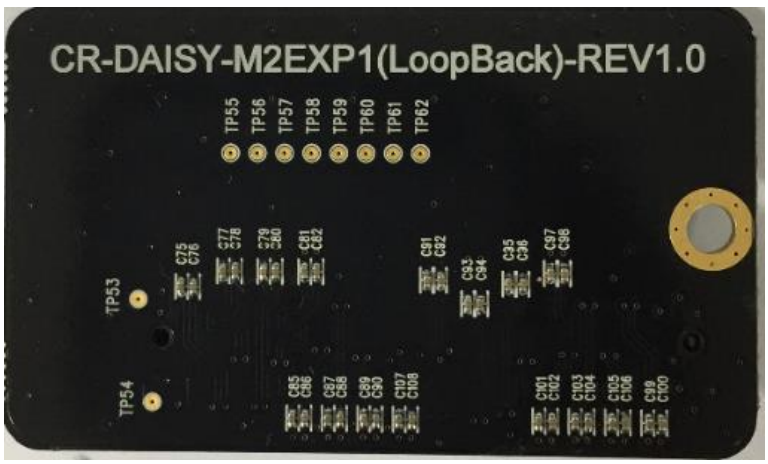


Figure 12. NVME M.2 Loopback Card

REF DES	Connector		Description
	Pin Name	Pin	
TP53	P_12V	53	12V power rail
TP54	VCC3V3	54	3.3V power rail

Table 10. Test points of NVME M.2 Loopback card

5. Clock system

5.1. 12-CH Clock Generator[U7]

Part Manufacturer : Silicon Labs

Part Number : SI5391

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U7	24	OUT0	GTR_REF_CLK0_100M_P	PS_MGTREFCLK0P_505_AG37	AG37	U1
	23	OUT0b	GTR_REF_CLK0_100M_N	PS_MGTREFCLK0N_505_AG38	AG38	
	21	OUT0A	GTR_REF_CLK1_108M_P	PS_MGTREFCLK1P_505_AE37	AE37	
	20	OUT0Ab	GTR_REF_CLK1_108M_N	PS_MGTREFCLK1N_505_AE38	AE38	
	28	OUT1	GTR_REF_CLK2_125M_P	PS_MGTREFCLK2P_505_AC37	AC37	
	27	OUT1b	GTR_REF_CLK2_125M_N	PS_MGTREFCLK2N_505_AC38	AC38	
	31	OUT2	GTR_REF_CLK3_150M_P	PS_MGTREFCLK3P_505_AA37	AA37	
	30	OUT2b	GTR_REF_CLK3_150M_N	PS_MGTREFCLK3N_505_AA38	AA38	
	35	OUT3	PL_DDR4_0_CLK_300MHZ_P	IO_L11P_T1U_N8_GC_64_AU21	AU21	
	34	OUT3b	PL_DDR4_0_CLK_300MHZ_N	IO_L11N_T1U_N9_GC_64_AV21	AV21	
	38	OUT4	PL_HD_BANK_CLK_P	IO_L5N_HDGC_AD7N_93_G7	G7	
	37	OUT4b	PL_HD_BANK_CLK_N	IO_L5P_HDGC_AD7P_93_F7	F7	
	42	OUT5	B128_REFCLK1P	MGTREFCLK0P_128_AB34	AB34	
	41	OUT5b	B128_REFCLK1N	MGTREFCLK0N_128_AB35	AB35	
	45	OUT6	B129_REFCLK1P	MGTREFCLK0P_129_W32	W32	
	44	OUT6b	B129_REFCLK1N	MGTREFCLK0N_129_W33	W33	
	51	OUT7	B130_REFCLK1P	MGTREFCLK0P_130_R32	R32	
	50	OUT7b	B130_REFCLK1N	MGTREFCLK0N_130_R33	R33	
	54	OUT8	B131_REFCLK1P	MGTREFCLK0P_131_L32	L32	
	53	OUT8b	B131_REFCLK1N	MGTREFCLK0N_131_L33	L33	
	56	OUT9	PL_DDR4_1_CLK_300MHZ_P	IO_L13P_T2L_N0_GC_QBC_70_G26	G26	
	55	OUT9b	PL_DDR4_1_CLK_300MHZ_N	IO_L13N_T2L_N1_GC_QBC_70_G27	G27	

Table 11. Signal assignment of 12-CH CLK Generator [U7]

5.2. 12-CH Clock Generator[U8]

Part Manufacturer : Silicon Labs

Part Number : SI5391

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U8	23	OUT0b	B224_REFCLK_N	MGTREFCLK0N_224_AK11	AK11	U1
	24	OUT0	B224_REFCLK_p	MGTREFCLK0P_224_AK12	AK12	
	20	OUT0Ab	B225_REFCLK_N	MGTREFCLK0N_225_AH11	AH11	
	21	OUT0A	B225_REFCLK_P	MGTREFCLK0P_225_AH12	AH12	
	27	OUT1b	B226_REFCLK_N	MGTREFCLK0N_226_AF11	AF11	
	28	OUT1	B226_REFCLK_P	MGTREFCLK0P_226_AF12	AF12	
	30	OUT2b	B227_REFCLK_N	MGTREFCLK0N_227_AD11	AD11	
	31	OUT2	B227_REFCLK_P	MGTREFCLK0P_227_AD12	AD12	
	34	OUT3b	B228_REFCLK_N	MGTREFCLK0N_228_AB11	AB11	
	35	OUT3	B228_REFCLK_P	MGTREFCLK0P_228_AB12	AB12	
	41	OUT5b	B229_REFCLK_N	MGTREFCLK0N_229_Y11	Y11	
	42	OUT5	B229_REFCLK_P	MGTREFCLK0P_229_Y12	Y12	
	50	OUT7b	B230_REFCLK_N	MGTREFCLK0N_230_V11	V11	
	51	OUT7	B230_REFCLK_P	MGTREFCLK0P_230_V12	V12	
	55	OUT9b	B231_REFCLK_N	MGTREFCLK0N_231_T11	T11	
	56	OUT9	B231_REFCLK_P	MGTREFCLK0P_231_T12	T12	
	37	OUT4b	EXP_B228_REFCLK_N	B_B228_CLKN	35	J25
	38	OUT4	EXP_B228_REFCLK_P	B_B228_CLKP	33	
	44	OUT6b	EXP_B229_REFCLK_N	36	36	
	45	OUT6	EXP_B229_REFCLK_P	34	34	
	53	OUT8b	EXP_B230_REFCLK_N	B_B230_CLKN	107	
	54	OUT8	EXP_B230_REFCLK_P	B_B230_CLKP	105	
	58	OUT9Ab	EXP_B231_REFCLK_N	108	108	
	59	OUT9A	EXP_B231_REFCLK_P	106	106	

Table 12. Signal assignment of 12-CH CLK Generator[U8]

6. MPSoC System Connections

6.1. NOR Flash 1GBIT [U9, U10]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	AM33	PS_MIO0_AM33	QSPI_LWR_CS_B	S_N	7	U9
	AM29	PS_MIO1_AM29	QSPI_LWR_CLK	C	16	
	AM31	PS_MIO2_AM31	QSPI_LWR_DQ1	DQ1	8	
	AM30	PS_MIO3_AM30	QSPI_LWR_DQ2	W_N/VPP/DQ2	9	
	AL33	PS_MIO4_AL33	QSPI_LWR_DQ3	HOLD_N/DQ3	1	
	AL32	PS_MIO5_AL32	QSPI_LWR_DQ0	DQ0	15	
	AL30	PS_MIO10_AK30	QSPI_UPR_CS_B	S_N	7	U10
	AK33	PS_MIO11_AK32	QSPI_UPR_CLK	C	16	
	AK34	PS_MIO12_AJ34	QSPI_UPR_DQ0	DQ1	8	
	AK30	PS_MIO7_AL30	QSPI_UPR_DQ1	W_N/VPP/DQ2	9	
	AK32	PS_MIO8_AK33	QSPI_UPR_DQ2	HOLD_N/DQ3	1	
	AJ34	PS_MIO9_AK34	QSPI_UPR_DQ3	DQ0	15	

Table 13. Signal assignment of NOR Flash 1GBIT [U9, U10]

6.2. Dual NVME M.2

6.2.1. NVME0[J25]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	AD4	MGTHRXP0_228_AD4	B228_RX0P	PERP0	9	J25
	AD3	MGTHRXN0_228_AD3	B228_RX0N	PERN0	11	
	AC2	MGTHRXP1_228_AC2	B228_RX1P	PERP1	15	
	AC1	MGTHRXN1_228_AC1	B228_RX1N	PERN1	17	
	AB4	MGTHRXP2_228_AB4	B228_RX2P	PERP2	21	
	AB3	MGTHRXN2_228_AB3	B228_RX2N	PERN2	23	
	AA2	MGTHRXP3_228_AA2	B228_RX3P	PERP3	27	
	AA1	MGTHRXN3_228_AA1	B228_RX3N	PERN3	29	
	AC6	MGTHTXP0_228_AC6	B228_TX0P	PETP0	10	

	AC5	MGTHTXN0_228_AC5	B228_TX0N	PETN0	12	
	AB8	MGTHTXP1_228_AB8	B228_TX1P	PETP1	16	
	AB7	MGTHTXN1_228_AB7	B228_TX1N	PETN1	18	
	AA6	MGTHTXP2_228_AA6	B228_TX2P	PETP2	22	
	AA5	MGTHTXN2_228_AA5	B228_TX2N	PETN2	24	
	Y8	MGTHTXP3_228_Y8	B228_TX3P	PETP3	28	
	Y7	MGTHTXN3_228_Y7	B228_TX3N	PETN3	30	
U8	38	OUT4	EXP_B228_REFCLK_P	REFCLKP	33	
	37	OUT4b	EXP_B228_REFCLK_N	REFCLKN	35	
U1	AB12	MGTREFCLK0P_228_AB12	B228_REFCLK_P	OUT3	35	**U8**
	AB11	MGTREFCLK0N_228_AB11	B228_REFCLK_N	OUT3b	34	
	B3	IO_L10P_AD10P_94_B3	GT_EXP_1_IO4	PERSTn	64	**J25**
	D4	IO_L5P_HDGC_94_D4	GT_EXP_1_IO14	CONFIG_1	76	

Table 14. Signal assignment of NVME0 M.2 [J25]

6.2.2. NVME1[J25]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	T4	MGTHRXP0_230_T4	B230_RX0P	PERP0	81	**J25**
	T3	MGTHRXN0_230_T3	B230_RX1P	PERN0	83	
	R2	MGTHRXP1_230_R2	B230_RX0N	PERP1	87	
	R1	MGTHRXN1_230_R1	B230_RX2P	PERN1	89	
	P4	MGTHRXP2_230_P4	B230_RX1N	PERP2	93	
	P3	MGTHRXN2_230_P3	B230_RX2N	PERN2	95	
	N2	MGTHRXP3_230_N2	B230_RX3N	PERP3	99	
	N1	MGTHRXN3_230_N1	B230_RX3P	PERN3	101	
	R6	MGTHTXP0_230_R6	B230_TX0P	PETP0	82	
	R5	MGTHTXN0_230_R5	B230_TX0N	PETN0	84	
	P8	MGTHTXP1_230_P8	B230_TX1P	PETP1	88	
	P7	MGTHTXN1_230_P7	B230_TX1N	PETN1	90	
	N6	MGTHTXP2_230_N6	B230_TX2P	PETP2	94	
	N5	MGTHTXN2_230_N5	B230_TX2N	PETN2	96	
	M8	MGTHTXP3_230_M8	B230_TX3P	PETP3	100	

	M7	MGTHTXN3_230_M7	B230_TX3N	PETN3	102	
U8	54	OUT8	EXP_B230_REFCLK_P	REFCLKP	105	
	53	OUT8b	EXP_B230_REFCLK_N	REFCLKN	107	
U1	V12	MGTREFCLK0P_230_V12	B230_REFCLK_P	OUT7	5	U8
	V11	MGTREFCLK0N_230_V11	B230_REFCLK_N	OUT7b	50	
	A3	IO_L10N_AD10N_94_A3	GT_EXP_1_IO5	PERSTn	66	J25
	D3	IO_L5N_HDGC_94_D3	GT_EXP_1_IO15	CONFIG_1	78	

Table 15. Signal assignment of NVME1 M.2 [J25]

6.3. QSFP28 100G Ethernet

6.3.3. QSFP0 [J20]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	N29	PS_MIO35_N29	QSFP1_MODSELL	MODSELL	8	J20
	T27	PS_MIO36_T27	QSFP1_RESETL	RESETL	9	
	N30	PS_MIO37_N30	QSFP1_MODPRSL	MODPRSL	27	
	R27	PS_MIO38_R27	QSFP1_INTL	INTL	28	
	P29	PS_MIO39_P29	QSFP1_LPMODE	LPMODE	31	
	AJ32	PS_MIO14_AJ32	PS_I2C0_SCL	SCL	11	
	AD35	PS_MIO15_AD35	PS_I2C0_SDA	SDA	12	
	L41	MGTYRXP0_130_L41	QSFP1_RX1_P	RX1P	17	
	L42	MGTYRXN0_130_L42	QSFP1_RX1_N	RX1N	18	
	K39	MGTYRXP1_130_K39	QSFP1_RX2_P	RX2P	22	
	K40	MGTYRXN1_130_K40	QSFP1_RX2_N	RX2N	21	
	J41	MGTYRXP2_130_J41	QSFP1_RX3_P	RX3P	14	
	J42	MGTYRXN2_130_J42	QSFP1_RX3_N	RX3N	15	
	H39	MGTYRXP3_130_H39	QSFP1_RX4_P	RX4P	25	
	H40	MGTYRXN3_130_H40	QSFP1_RX4_N	RX4N	24	
	M34	MGTYTXP0_130_M34	QSFP1_TX1_P	TX1P	36	
	M35	MGTYTXN0_130_M35	QSFP1_TX1_N	TX1N	37	
	L36	MGTYTXP1_130_L36	QSFP1_TX2_P	TX2P	3	
	L37	MGTYTXN1_130_L37	QSFP1_TX2_N	TX2N	2	
	K34	MGTYTXP2_130_K34	QSFP1_TX3_P	TX3P	33	

	K35	MGTYTXN2_130_K35	QSFP1_TX3_N	TX3N	34	
	J36	MGTYTXP3_130_J36	QSFP1_TX4_P	TX4P	6	
	J37	MGTYTXN3_130_J37	QSFP1_TX4_N	TX4N	5	

Table 16. Signal assignment of QSFP0 [J20]

6.3.4. QSFP1 [J23]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	P28	PS_MIO40_P28	QSFP2_LPMODE	MODSELL	8	J23
	P30	PS_MIO41_P30	QSFP2_RESETL	RESETL	9	
	T30	PS_MIO42_T30	QSFP2_MODSELL	MODPRSL	27	
	R30	PS_MIO43_R30	QSFP2_INTL	INTL	28	
	R29	PS_MIO44_R29	QSFP2_MODPRSL	LPMODE	31	
	AJ31	PS_MIO16_AJ31	PS_I2C1_SCL	SCL	11	
	AJ30	PS_MIO17_AJ30	PS_I2C1_SDA	SDA	12	
	G41	MGTYRXP0_131_G41	QSFP2_RX1_P	RX1P	17	
	G42	MGTYRXN0_131_G42	QSFP2_RX1_N	RX1N	18	
	F39	MGTYRXP1_131_F39	QSFP2_RX2_P	RX2P	22	
	F40	MGTYRXN1_131_F40	QSFP2_RX2_N	RX2N	21	
	E41	MGTYRXP2_131_E41	QSFP2_RX3_P	RX3P	14	
	E42	MGTYRXN2_131_E42	QSFP2_RX3_N	RX3N	15	
	D39	MGTYRXP3_131_D39	QSFP2_RX4_P	RX4P	25	
	D40	MGTYRXN3_131_D40	QSFP2_RX4_N	RX4N	24	
	H34	MGTYTXP0_131_H34	QSFP2_TX1_P	TX1P	36	
	H35	MGTYTXN0_131_H35	QSFP2_TX1_N	TX1N	37	
	G36	MGTYTXP1_131_G36	QSFP2_TX2_P	TX2P	3	
	G37	MGTYTXN1_131_G37	QSFP2_TX2_N	TX2N	2	
	F34	MGTYTXP2_131_F34	QSFP2_TX3_P	TX3P	33	
	F35	MGTYTXN2_131_F35	QSFP2_TX3_N	TX3N	34	
	E36	MGTYTXP3_131_E36	QSFP2_TX4_P	TX4P	6	
	E37	MGTYTXN3_131_E37	QSFP2_TX4_N	TX4N	5	

Table 17. Signal assignment of QSFP1 [J23]

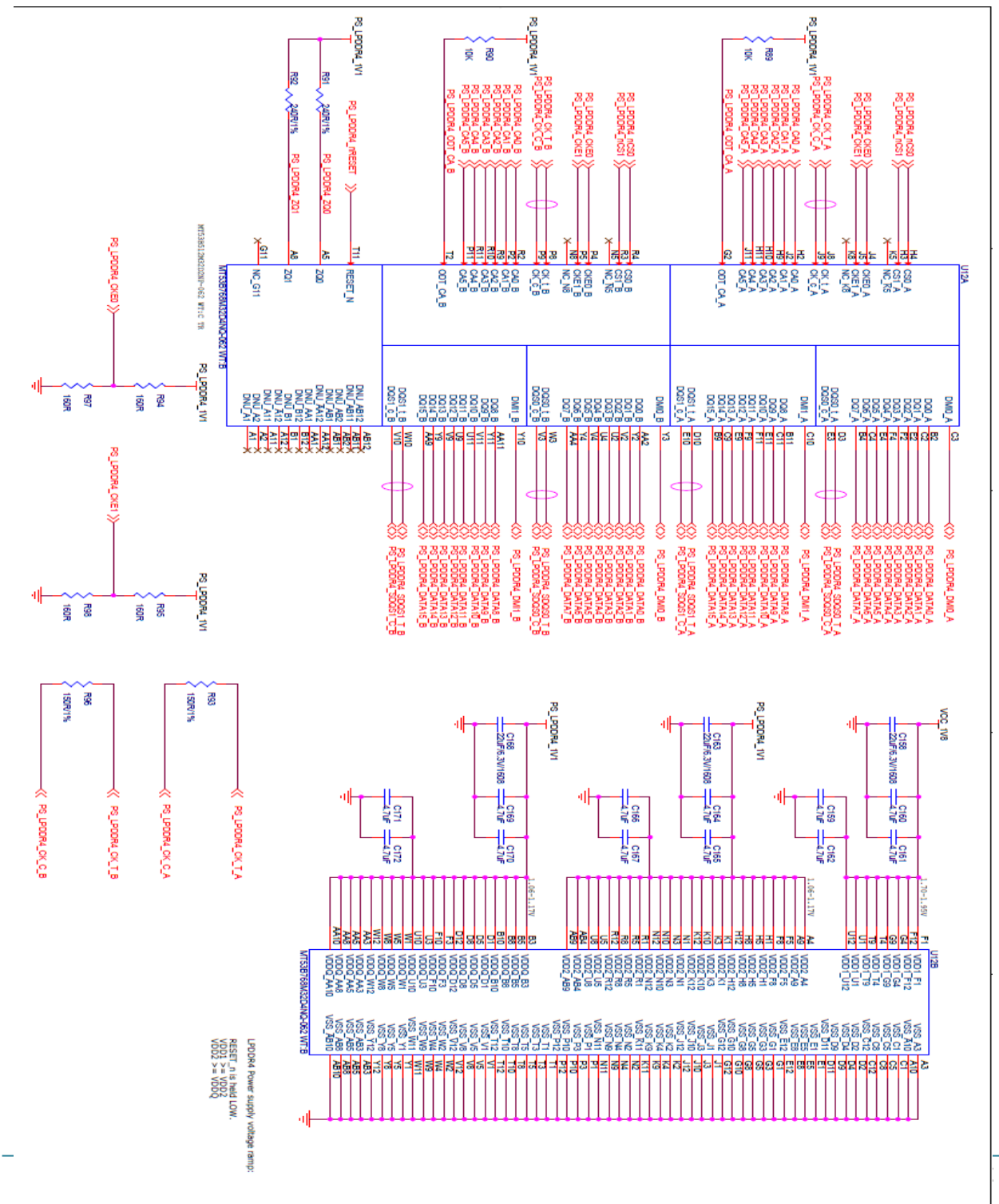
6.4. PS LPDDR4 [U12]

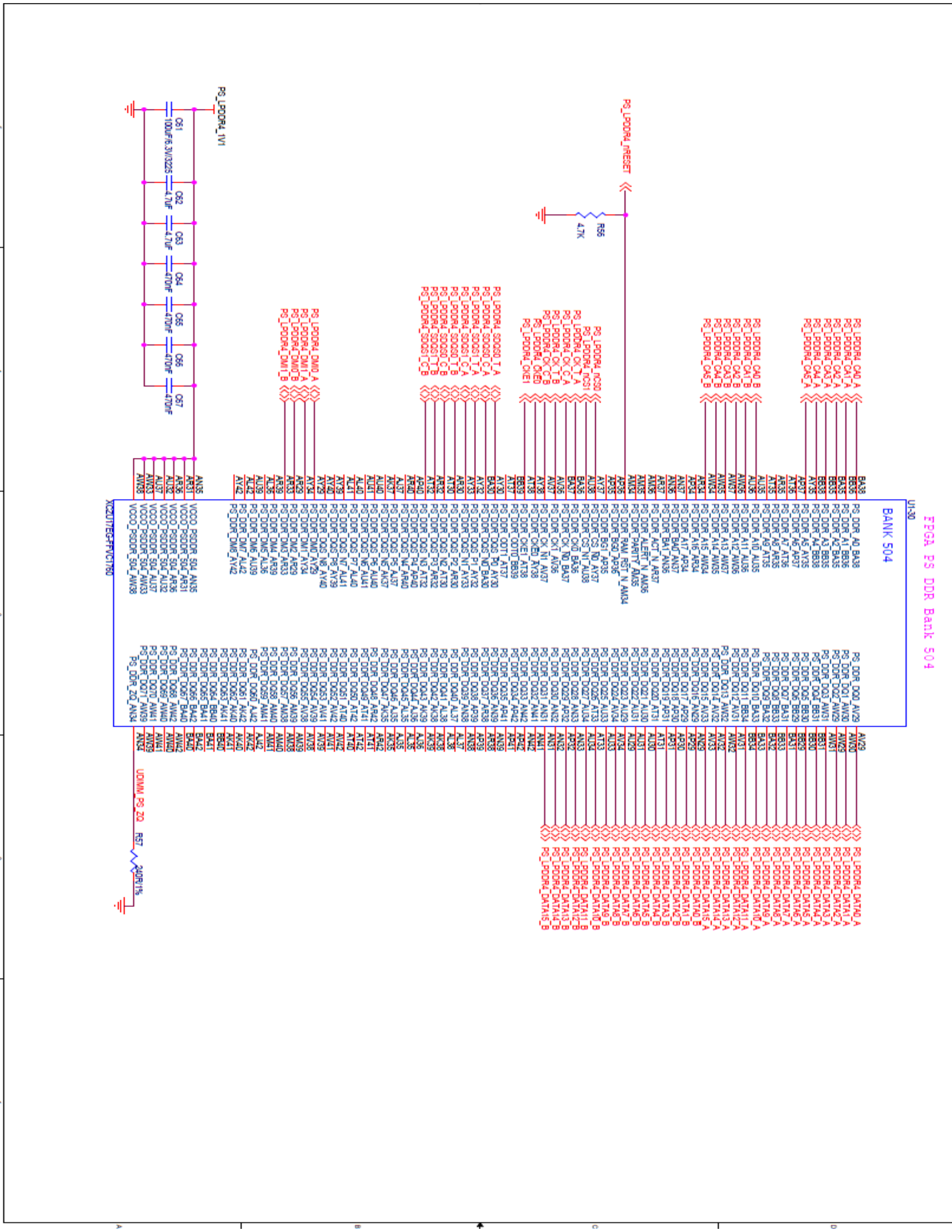
Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1 (XCZU17EG -FFVC1760)	BA38	PS_DDR_A0_BA38	PS_LPDDR4_CA0_A	CA0_A	H2	U12 (MT53B768M32D4NQ -062)
	BB36	PS_DDR_A1_BB36	PS_LPDDR4_CA1_A	CA1_A	J2	
	BA35	PS_DDR_A2_BA35	PS_LPDDR4_CA2_A	CA2_A	H9	
	BB35	PS_DDR_A3_BB35	PS_LPDDR4_CA3_A	CA3_A	H10	
	BB38	PS_DDR_A4_BB38	PS_LPDDR4_CA4_A	CA4_A	H11	
	AY35	PS_DDR_A5_AY35	PS_LPDDR4_CA5_A	CA5_A	J11	
	AU35	PS_DDR_A10_AU35	PS_LPDDR4_CA0_B	CA0_B	R2	
	AU36	PS_DDR_A11_AU36	PS_LPDDR4_CA1_B	CA1_B	P2	
	AW36	PS_DDR_A12_AW36	PS_LPDDR4_CA2_B	CA2_B	R9	
	AW37	PS_DDR_A13_AW37	PS_LPDDR4_CA3_B	CA3_B	R10	
	AW35	PS_DDR_A14_AW35	PS_LPDDR4_CA4_B	CA4_B	R11	
	AW34	PS_DDR_A15_AW34	PS_LPDDR4_CA5_B	CA5_B	P11	
	AM34	S_DDR_RAM_RST_N_AM34	PS_LPDDR4_nRESET	RESET_N	T11	
	AY37	PS_DDR_CS_N0_AY37	PS_LPDDR4_nCS0	CS0_B	R4	
	AU38	PS_DDR_CS_N1_AU38	PS_LPDDR4_nCS1	CS1_B	R3	
	BA36	PS_DDR_CK0_BA36	PS_LPDDR4_CK_T_A	CK_t_A	J8	
	BA37	PS_DDR_CK_N0_BA37	PS_LPDDR4_CK_C_A	CK_c_A	J9	
	AV36	PS_DDR_CK1_AV36	PS_LPDDR4_CK_T_B	CK_t_B	P8	
	AV37	PS_DDR_CK_N1_AV37	PS_LPDDR4_CK_C_B	CK_c_B	P9	
	AY38	PS_DDR_CKE0_AY38	PS_LPDDR4_CKE0	CKE0_B	P4	
	AT38	PS_DDR_CKE1_AT38	PS_LPDDR4_CKE1	CKE1_B	P5	
	AY30	PS_DDR_DQS_P0_AY30	PS_LPDDR4_SDQS0_T_A	DQS0_t_A	D3	
	BA30	PS_DDR_DQS_N0_BA30	PS_LPDDR4_SDQS0_C_A	DQS0_c_A	E3	
	AY32	PS_DDR_DQS_P1_AY32	PS_LPDDR4_SDQS1_T_A	DQS1_t_A	D10	
	AY33	PS_DDR_DQS_N1_AY33	PS_LPDDR4_SDQS1_C_A	DQS1_c_	E10	

				A		
	AR30	PS_DDR_DQS_P2_AR30	PS_LPDDR4_SDQS0_T_B	DQS0_t_B	W3	
	AT30	PS_DDR_DQS_N2_AT30	PS_LPDDR4_SDQS0_C_B	DQS0_c_B	V3	
	AR32	PS_DDR_DQS_P3_AR32	PS_LPDDR4_SDQS1_T_B	DQS1_t_B	W10	
	AT32	PS_DDR_DQS_N3_AT32	PS_LPDDR4_SDQS1_C_B	DQS1_c_B	V10	
	AY29	PS_DDR_DM0_AY29	PS_LPDDR4_DMI0_A	DMI0_A	C3	
	AY34	PS_DDR_DM1_AY34	PS_LPDDR4_DMI1_A	DMI1_A	C10	
	AR29	PS_DDR_DM2_AR29	PS_LPDDR4_DMI0_B	DMI0_B	Y3	
	AR33	PS_DDR_DM3_AR33	PS_LPDDR4_DMI1_B	DMI1_B	Y10	
	AV29	PS_DDR_DQ0_AV29	PS_LPDDR4_DATA0_A	DQ0_A	B2	
	AW30	PS_DDR_DQ1_AW30	PS_LPDDR4_DATA1_A	DQ1_A	C2	
	AW29	PS_DDR_DQ2_AW29	PS_LPDDR4_DATA2_A	DQ2_A	E2	
	AW31	PS_DDR_DQ3_AW31	PS_LPDDR4_DATA3_A	DQ3_A	F2	
	BB31	PS_DDR_DQ4_BB31	PS_LPDDR4_DATA4_A	DQ4_A	F4	
	BB30	PS_DDR_DQ5_BB30	PS_LPDDR4_DATA5_A	DQ5_A	E4	
	BB29	PS_DDR_DQ6_BB29	PS_LPDDR4_DATA6_A	DQ6_A	C4	
	BA31	PS_DDR_DQ7_BA31	PS_LPDDR4_DATA7_A	DQ7_A	B4	
	BB33	PS_DDR_DQ8_BB33	PS_LPDDR4_DATA8_A	DQ8_A	B11	
	BA32	PS_DDR_DQ9_BA32	PS_LPDDR4_DATA9_A	DQ9_A	C11	
	BA33	PS_DDR_DQ10_BA33	PS_LPDDR4_DATA10_A	DQ10_A	E11	
	BB34	PS_DDR_DQ11_BB34	PS_LPDDR4_DATA11_A	DQ11_A	F11	
	AV31	PS_DDR_DQ12_AV31	PS_LPDDR4_DATA12_A	DQ12_A	F9	
	AW32	PS_DDR_DQ13_AW32	PS_LPDDR4_DATA13_A	DQ13_A	E9	
	AV32	PS_DDR_DQ14_AV32	PS_LPDDR4_DATA14_A	DQ14_A	C9	
	AV33	PS_DDR_DQ15_AV33	PS_LPDDR4_DATA15_A	DQ15_A	B9	
	AN29	PS_DDR_DQ16_AN29	PS_LPDDR4_DATA1_B	DQ0_B	AA2	
	AP29	PS_DDR_DQ17_AP29	PS_LPDDR4_DATA1_B	DQ1_B	Y2	
	AP30	PS_DDR_DQ18_AP30	PS_LPDDR4_DATA2_B	DQ2_B	V2	
	AP31	PS_DDR_DQ19_AP31	PS_LPDDR4_DATA3_B	DQ3_B	U2	

	AT31	PS_DDR_DQ20_AT31	PS_LPDDR4_DATA4_B	DQ4_B	U4	
	AU30	PS_DDR_DQ21_AU30	PS_LPDDR4_DATA5_B	DQ5_B	V4	
	AU31	PS_DDR_DQ22_AU31	PS_LPDDR4_DATA6_B	DQ6_B	Y4	
	AU29	PS_DDR_DQ23_AU29	PS_LPDDR4_DATA7_B	DQ7_B	AA4	
	AV34	PS_DDR_DQ24_AV34	PS_LPDDR4_DATA8_B	DQ8_B	AA11	
	AU33	PS_DDR_DQ25_AU33	PS_LPDDR4_DATA9_B	DQ9_B	Y11	
	AT33	PS_DDR_DQ26_AT33	PS_LPDDR4_DATA10_B	DQ10_B	V11	
	AU34	PS_DDR_DQ27_AU34	PS_LPDDR4_DATA11_B	DQ11_B	U11	
	AN33	PS_DDR_DQ28_AN33	PS_LPDDR4_DATA12_B	DQ12_B	U9	
	AP32	PS_DDR_DQ29_AP32	PS_LPDDR4_DATA13_B	DQ13_B	V9	
	AN32	PS_DDR_DQ30_AN32	PS_LPDDR4_DATA14_B	DQ14_B	Y9	
	AN31	PS_DDR_DQ31_AN31	PS_LPDDR4_DATA15_B	DQ15_B	AA9	

Table 18. Signal assignment of PS LPDDR4 [U12]


U12A
U12B
MT53B512M32D2NP-062 WT:B
PG_LPDDR4_1V1
PG_LPDDR4_DMI0_A
PG_LPDDR4_DMI1_A
PG_LPDDR4_DMI0_B
PG_LPDDR4_DMI1_B
PG_LPDDR4_CK_T_A
PG_LPDDR4_CK_C_A
PG_LPDDR4_CK_T_B
PG_LPDDR4_CK_C_B
PG_LPDDR4_CKE0
PG_LPDDR4_CKE1
PG_LPDDR4_RESET
VCC_1V8
RESET_n is held LOW.
VDD1 >= VDD2


FPGA PS DDR Bank 504
BANK 504
PS_LPDDR4_1V1

6.5. PL DIMM Card Slots

6.5.1. DIMM0 [J8]

Device	Pin	Pin Name	Schematic Net Name	Pin	Device
U1 (XCZU17EG-FFVC1760)	AW19	IO_L9N_T1L_N5_AD12N_64_AW19	DDR4_0_RTL_ODT0	87	J8
	BA18	IO_L6P_T0U_N10_AD6P_64_BA18	DDR4_0_RTL_ODT1	91	
	AT20	IO_L14P_T2L_N2_GC_64_AT20	DDR4_0_RTL_PAR	222	
	AP22	IO_L15N_T2L_N5_AD11N_64_AP22	DDR4_0_RTL_RESET_N	58	
	AV23	IO_L7N_T1L_N1_QBC_AD13N_64_AV23	DDR4_0_RTL_ACT_N	62	
	BB23	IO_L1N_T0L_N1_DBC_64_BB23	DDR4_0_RTL_ALERT_B	208	
	AP19	IO_L18P_T2U_N10_AD2P_64_AP19	DDR4_0_RTL_BA0	81	
	AV19	IO_L12N_T1U_N11_GC_64_AV19	DDR4_0_RTL_BA1	224	
	AY23	IO_L2P_T0L_N2_64_AY23	DDR4_0_RTL_BG0	63	
	AV22	IO_L8P_T1L_N2_AD5P_64_AV22	DDR4_0_RTL_BG1	207	
	AR22	IO_T2U_N12_64_AR22	DDR4_0_RTL_CKE0	60	
	AU23	IO_L7P_T1L_N0_QBC_AD13P_64_AU23	DDR4_0_RTL_CKE1	203	
	BA20	IO_L4N_T0U_N7_DBC_AD7N_64_BA20	DDR4_0_RTL_CK_C0	75	
	AY20	IO_L4P_T0U_N6_DBC_AD7P_64_AY20	DDR4_0_RTL_CK_T0	74	
	AW20	IO_L9P_T1L_N4_AD12P_64_AW20	DDR4_0_RTL_CS_N0	84	
	AY18	IO_L10N_T1U_N7_QBC_AD4N_64_AY18	DDR4_0_RTL_CS_N1	89	
	AJ32	PS_MIO14_AJ32	PS_I2C0_SCL	141	
	AD35	PS_MIO15_AD35	PS_I2C0_SDA	285	
	AU19	IO_L14N_T2L_N3_GC_64_AU19	DDR4_0_RTL_EVENT_B	78	
	AR19	IO_L18N_T2U_N11_AD2N_64_AR19	DDR4_0_RTL_ADR0	79	
	AR20	IO_L17N_T2U_N9_AD10N_64_AR20	DDR4_0_RTL_ADR1	72	
	AP20	IO_L17P_T2U_N8_AD10P_64_AP20	DDR4_0_RTL_ADR2	216	
	AP21	L16N_T2U_N7_QBC_AD3N_64_AP21	DDR4_0_RTL_ADR3	71	
	BA22	IO_L3P_T0L_N4_AD15P_64_BA22	DDR4_0_RTL_ADR4	214	
	AW22	IO_L8N_T1L_N3_AD5N_64_AW22	DDR4_0_RTL_ADR5	213	
	AT21	IO_L13N_T2L_N1_GC_QBC_64_AT21	DDR4_0_RTL_ADR6	69	
	AY22	IO_L2N_T0L_N3_64_AY22	DDR4_0_RTL_ADR7	211	
	AN21	IO_L16P_T2U_N6_QBC_AD3P_64_AN21	DDR4_0_RTL_ADR8	68	
	AN22	IO_L15P_T2L_N4_AD11P_64_AN22	DDR4_0_RTL_ADR9	66	
	BA21	IO_L3N_T0L_N5_AD15N_64_BA21	DDR4_0_RTL_ADR10	225	
	BA23	IO_L1P_T0L_N0_DBC_64_BA23	DDR4_0_RTL_ADR11	210	

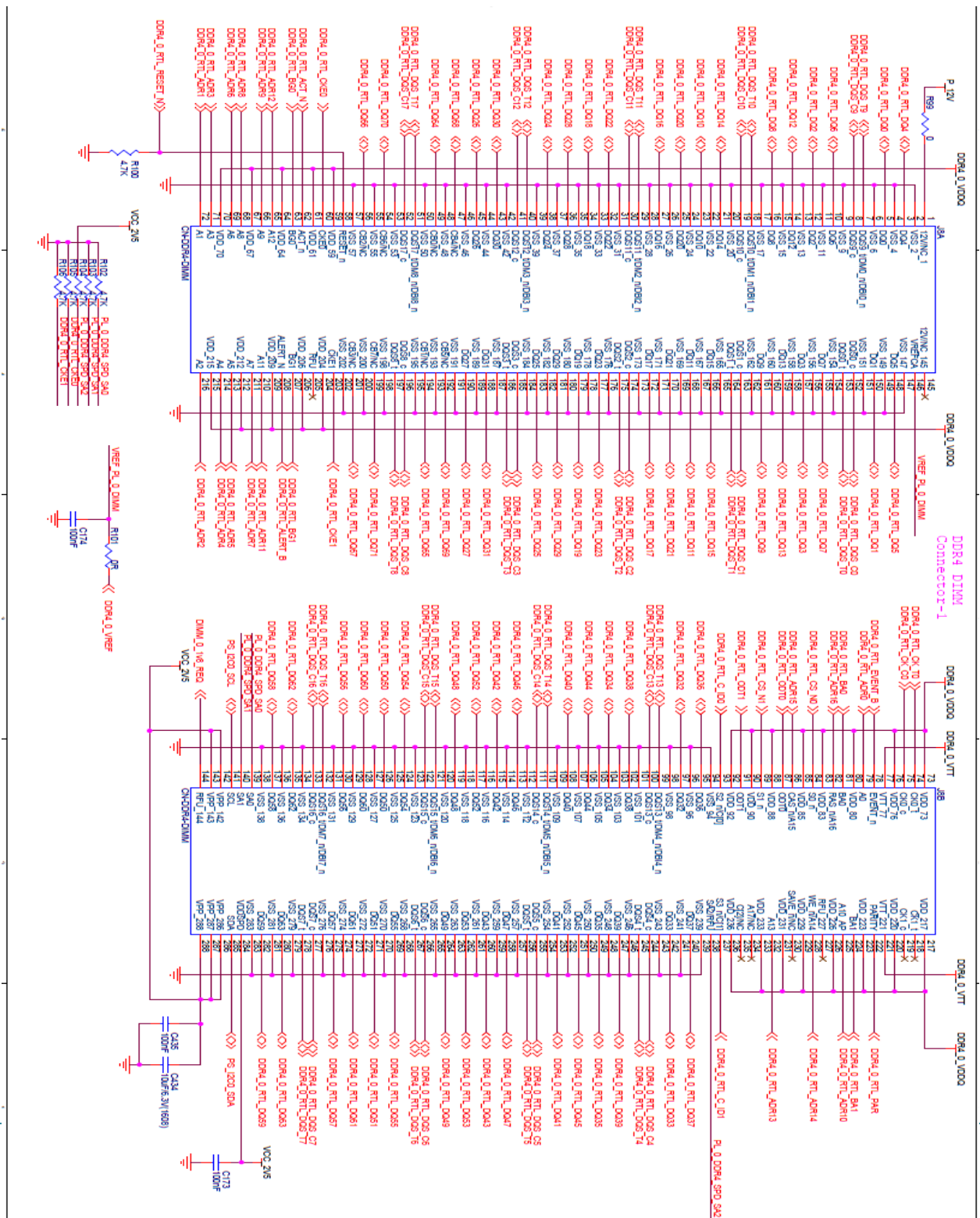
	AT22	IO_L13P_T2L_N0_GC_QBC_64_AT22	DDR4_0_RTL_ADR12	65	
	AY19	IO_L10P_T1U_N6_QBC_AD4P_64_AY19	DDR4_0_RTL_ADR13	232	
	BB20	IO_L5P_T0U_N8_AD14P_64_BB20	DDR4_0_RTL_ADR14	228	
	AU20	IO_L12P_T1U_N10_GC_64_AU20	DDR4_0_RTL_ADR15	86	
	AW21	IO_T1U_N12_64_AW21	DDR4_0_RTL_ADR16	82	
	AN27	IO_L16P_T2U_N6_QBC_AD3P_65_AN27	DDR4_0_RTL_DQS_T0	153	
	AP27	IO_L16N_T2U_N7_QBC_AD3N_65_AP27	DDR4_0_RTL_DQS_C0	152	
	AU28	IO_L10P_T1U_N6_QBC_AD4P_65_AU28	DDR4_0_RTL_DQS_T1	164	
	AV28	IO_L10N_T1U_N7_QBC_AD4N_65_AV28	DDR4_0_RTL_DQS_C1	163	
	BA26	IO_L4P_T0U_N6_DBC_AD7P_65_BA26	DDR4_0_RTL_DQS_T2	175	
	BB26	IO_L4N_T0U_N7_DBC_AD7N_65_BB26	DDR4_0_RTL_DQS_C2	174	
	AM23	IO_L22P_T3U_N6_DBC_AD0P_65_AM23	DDR4_0_RTL_DQS_T3	186	
	AN23	IO_L22N_T3U_N7_DBC_AD0N_65_AN23	DDR4_0_RTL_DQS_C3	185	
	BA15	IO_L4P_T0U_N6_DBC_AD7P_66_BA15	DDR4_0_RTL_DQS_T4	245	
	BB15	IO_L4N_T0U_N7_DBC_AD7N_66_BB15	DDR4_0_RTL_DQS_C4	244	
	AN12	IO_L16P_T2U_N6_QBC_AD3P_67_AN12	DDR4_0_RTL_DQS_T5	256	
	AP12	IO_L16N_T2U_N7_QBC_AD3N_67_AP12	DDR4_0_RTL_DQS_C5	255	
	AU13	IO_L10P_T1U_N6_QBC_AD4P_66_AU13	DDR4_0_RTL_DQS_T6	267	
	AV13	IO_L10N_T1U_N7_QBC_AD4N_66_AV13	DDR4_0_RTL_DQS_C6	266	
	BA8	IO_L4P_T0U_N6_DBC_AD7P_67_BA8	DDR4_0_RTL_DQS_T7	278	
	BA7	IO_L4N_T0U_N7_DBC_AD7N_67_BA7	DDR4_0_RTL_DQS_C7	277	
	AK20	IO_L22P_T3U_N6_DBC_AD0P_64_AK20	DDR4_0_RTL_DQS_T8	197	
	AK19	IO_L22N_T3U_N7_DBC_AD0N_64_AK19	DDR4_0_RTL_DQS_C8	196	
	AR27	IO_L13P_T2L_N0_GC_QBC_65_AR27	DDR4_0_RTL_DQS_T9	7	
	AT27	IO_L13N_T2L_N1_GC_QBC_65_AT27	DDR4_0_RTL_DQS_C9	8	
	AU24	IO_L7P_T1L_N0_QBC_AD13P_65_AU24	DDR4_0_RTL_DQS_T10	18	
	AV24	IO_L7N_T1L_N1_QBC_AD13N_65_AV24	DDR4_0_RTL_DQS_C10	19	
	AW24	IO_L1P_T0L_N0_DBC_65_AW24	DDR4_0_RTL_DQS_T11	29	
	AY24	IO_L1N_T0L_N1_DBC_65_AY24	DDR4_0_RTL_DQS_C11	30	
	AR23	IO_L19P_T3L_N0_DBC_AD9P_65_AR23	DDR4_0_RTL_DQS_T12	40	
	AT23	IO_L19N_T3L_N1_DBC_AD9N_65_AT23	DDR4_0_RTL_DQS_C12	41	
	AY17	IO_L1P_T0L_N0_DBC_66_AY17	DDR4_0_RTL_DQS_T13	99	
	BA17	IO_L1N_T0L_N1_DBC_66_BA17	DDR4_0_RTL_DQS_C13	100	
	AR13	IO_L13P_T2L_N0_GC_QBC_67_AR13	DDR4_0_RTL_DQS_T14	110	

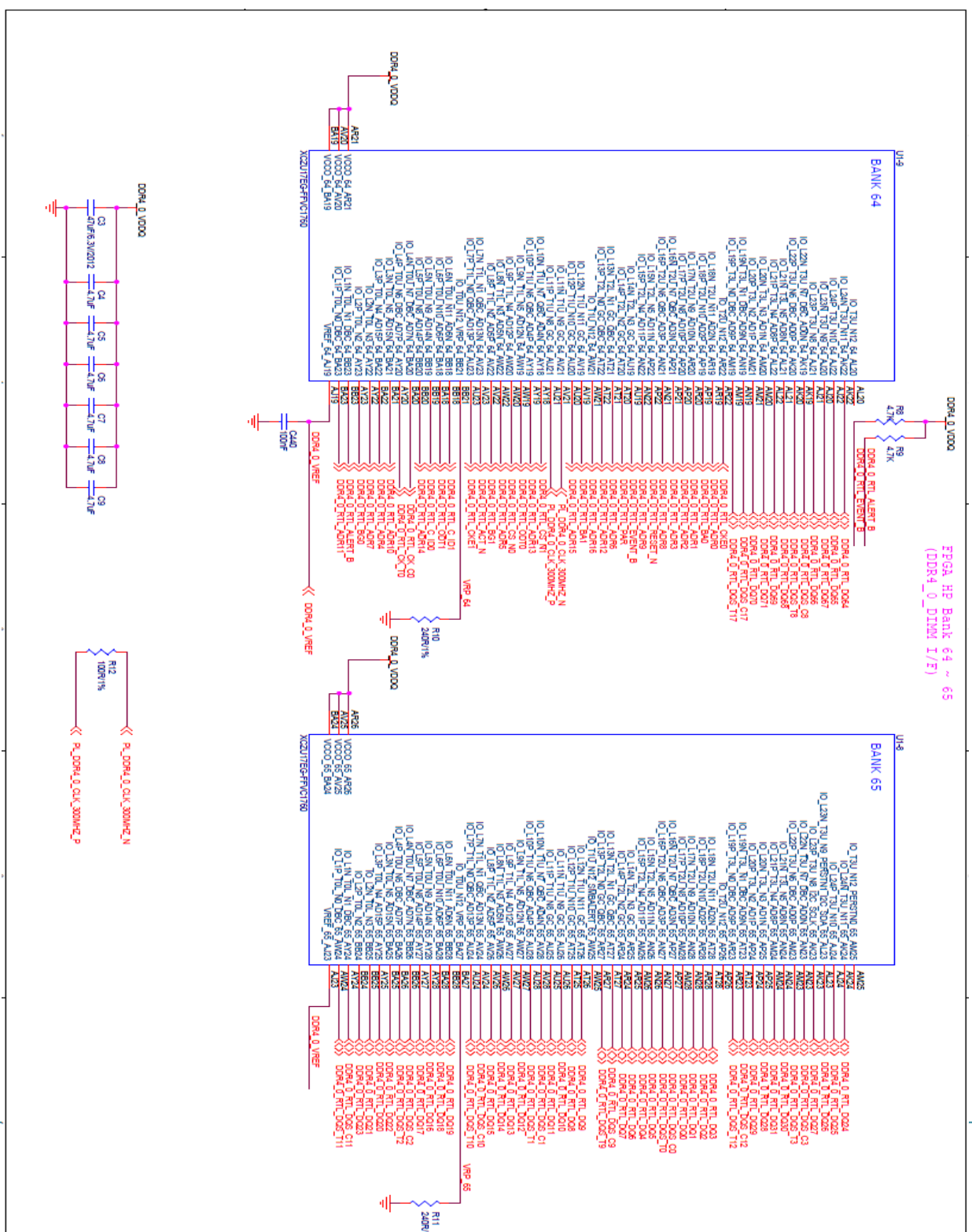
	AR12	IO_L13N_T2L_N1_GC_QBC_67_AR12	DDR4_0_RTL_DQS_C14	111	
	AY12	IO_L7P_T1L_N0_QBC_AD13P_66_AY12	DDR4_0_RTL_DQS_T15	121	
	BA12	IO_L7N_T1L_N1_QBC_AD13N_66_BA12	DDR4_0_RTL_DQS_C15	122	
	AW9	IO_L1P_T0L_N0_DBC_67_AW9	DDR4_0_RTL_DQS_T16	132	
	AY9	IO_L1N_T0L_N1_DBC_67_AY9	DDR4_0_RTL_DQS_C16	133	
	AM19	IO_L19P_T3L_N0_DBC_AD9P_64_AM19	DDR4_0_RTL_DQS_T17	51	
	AN19	IO_L19N_T3L_N1_DBC_AD9N_64_AN19	DDR4_0_RTL_DQS_C17	52	
	AM28	IO_L17P_T2U_N8_AD10P_65_AM28	DDR4_0_RTL_DQ0	5	
	AN28	IO_L17N_T2U_N9_AD10N_65_AN28	DDR4_0_RTL_DQ1	150	
	AR28	IO_L18P_T2U_N10_AD2P_65_AR28	DDR4_0_RTL_DQ2	12	
	AT28	IO_L18N_T2U_N11_AD2N_65_AT28	DDR4_0_RTL_DQ3	157	
	AM26	IO_L15P_T2L_N4_AD11P_65_AM26	DDR4_0_RTL_DQ4	3	
	AN26	IO_L15N_T2L_N5_AD11N_65_AN26	DDR4_0_RTL_DQ5	148	
	AR25	IO_L14N_T2L_N3_GC_65_AR25	DDR4_0_RTL_DQ6	10	
	AR24	IO_L14P_T2L_N2_GC_65_AR24	DDR4_0_RTL_DQ7	155	
	AU26	IO_L11N_T1U_N9_GC_65_AU26	DDR4_0_RTL_DQ8	16	
	AT25	IO_L12P_T1U_N10_GC_65_AT25	DDR4_0_RTL_DQ9	161	
	AU25	IO_L11P_T1U_N8_GC_65_AU25	DDR4_0_RTL_DQ10	23	
	AT26	IO_L12N_T1U_N11_GC_65_AT26	DDR4_0_RTL_DQ11	168	
	AW27	IO_L9N_T1L_N5_AD12N_65_AW27	DDR4_0_RTL_DQ12	14	
	AV27	IO_L9P_T1L_N4_AD12P_65_AV27	DDR4_0_RTL_DQ13	159	
	AW26	IO_L8N_T1L_N3_AD5N_65_AW26	DDR4_0_RTL_DQ14	21	
	AV26	IO_L8P_T1L_N2_AD5P_65_AV26	DDR4_0_RTL_DQ15	166	
	AY28	IO_L5N_T0U_N9_AD14N_65_AY28	DDR4_0_RTL_DQ16	27	
	AY27	IO_L5P_T0U_N8_AD14P_65_AY27	DDR4_0_RTL_DQ17	172	
	BA28	IO_L6P_T0U_N10_AD6P_65_BA28	DDR4_0_RTL_DQ18	34	
	BB28	IO_L6N_T0U_N11_AD6N_65_BB28	DDR4_0_RTL_DQ19	179	
	AY25	IO_L3P_T0L_N4_AD15P_65_AY25	DDR4_0_RTL_DQ20	25	
	BB25	IO_L2N_T0L_N3_65_BB25	DDR4_0_RTL_DQ21	170	
	BA25	IO_L3N_T0L_N5_AD15N_65_BA25	DDR4_0_RTL_DQ22	32	
	BB24	IO_L2P_T0L_N2_65_BB24	DDR4_0_RTL_DQ23	177	
	AK24	IO_L24N_T3U_N11_65_AK24	DDR4_0_RTL_DQ24	38	
	AJ24	IO_L24P_T3U_N10_65_AJ24	DDR4_0_RTL_DQ25	183	
	AL23	IO_L23N_T3U_N9_PERSTN1_I2C_SDA_65_AL23	DDR4_0_RTL_DQ26	45	

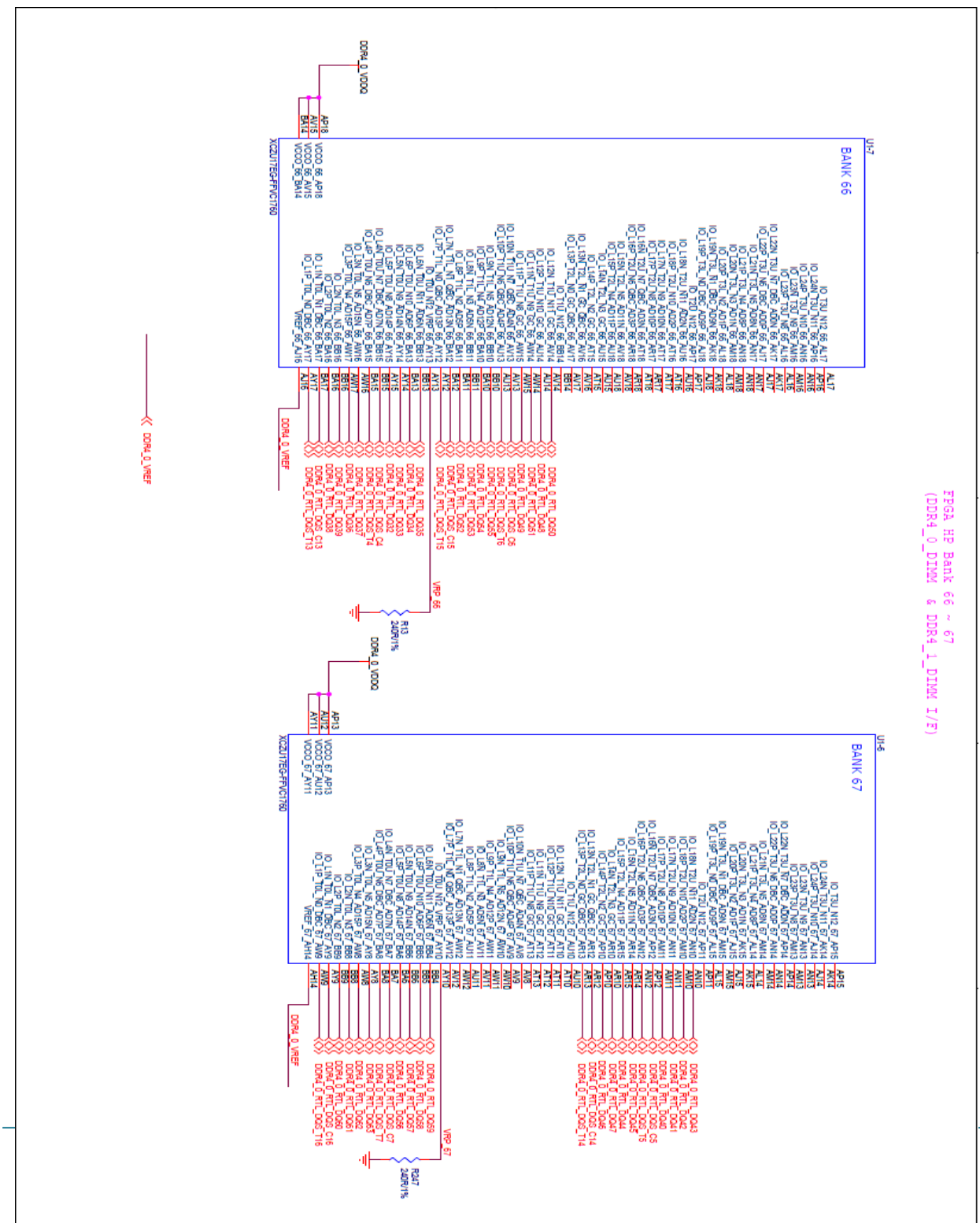
	AK23	IO_L23P_T3U_N8_I2C_SCLK_65_AK23	DDR4_0_RTL_DQ27	190	
	AP25	IO_L20N_T3L_N3_AD1N_65_AP25	DDR4_0_RTL_DQ28	36	
	AP24	IO_L20P_T3L_N2_AD1P_65_AP24	DDR4_0_RTL_DQ29	181	
	AN24	IO_L21N_T3L_N5_AD8N_65_AN24	DDR4_0_RTL_DQ30	43	
	AM24	IO_L21P_T3L_N4_AD8P_65_AM24	DDR4_0_RTL_DQ31	188	
	AY15	IO_L5P_T0U_N8_AD14P_66_AY15	DDR4_0_RTL_DQ32	97	
	AY14	IO_L5N_T0U_N9_AD14N_66_AY14	DDR4_0_RTL_DQ33	242	
	BA13	IO_L6P_T0U_N10_AD6P_66_BA13	DDR4_0_RTL_DQ34	104	
	BB13	IO_L6N_T0U_N11_AD6N_66_BB13	DDR4_0_RTL_DQ35	249	
	AW17	IO_L3P_T0L_N4_AD15P_66_AW17	DDR4_0_RTL_DQ36	95	
	AW16	IO_L3N_T0L_N5_AD15N_66_AW16	DDR4_0_RTL_DQ37	240	
	BA16	IO_L2P_T0L_N2_66_BA16	DDR4_0_RTL_DQ38	102	
	BB16	IO_L2N_T0L_N3_66_BB16	DDR4_0_RTL_DQ39	247	
	AM11	IO_L17P_T2U_N8_AD10P_67_AM11	DDR4_0_RTL_DQ40	108	
	AN11	IO_L17N_T2U_N9_AD10N_67_AN11	DDR4_0_RTL_DQ41	253	
	AM10	IO_L18P_T2U_N10_AD2P_67_AM10	DDR4_0_RTL_DQ42	115	
	AN10	IO_L18N_T2U_N11_AD2N_67_AN10	DDR4_0_RTL_DQ43	260	
	AR14	IO_L15N_T2L_N5_AD11N_67_AR14	DDR4_0_RTL_DQ44	106	
	AR15	IO_L15P_T2L_N4_AD11P_67_AR15	DDR4_0_RTL_DQ45	251	
	AP10	IO_L14P_T2L_N2_GC_67_AP10	DDR4_0_RTL_DQ46	113	
	AR10	IO_L14N_T2L_N3_GC_67_AR10	DDR4_0_RTL_DQ47	258	
	AU14	IO_L12P_T1U_N10_GC_66_AU14	DDR4_0_RTL_DQ48	119	
	AW15	IO_L11P_T1U_N8_GC_66_AW15	DDR4_0_RTL_DQ49	264	
	AV14	IO_L12N_T1U_N11_GC_66_AV14	DDR4_0_RTL_DQ50	126	
	AW14	IO_L11N_T1U_N9_GC_66_AW14	DDR4_0_RTL_DQ51	271	
	BA11	IO_L8P_T1L_N2_AD5P_66_BA11	DDR4_0_RTL_DQ52	117	
	BB11	IO_L8N_T1L_N3_AD5N_66_BB11	DDR4_0_RTL_DQ53	262	
	BA10	IO_L9P_T1L_N4_AD12P_66_BA10	DDR4_0_RTL_DQ54	124	
	BB10	IO_L9N_T1L_N5_AD12N_66_BB10	DDR4_0_RTL_DQ55	269	
	BA6	IO_L5P_T0U_N8_AD14P_67_BA6	DDR4_0_RTL_DQ56	130	
	BB6	IO_L5N_T0U_N9_AD14N_67_BB6	DDR4_0_RTL_DQ57	275	
	BB5	IO_L6P_T0U_N10_AD6P_67_BB5	DDR4_0_RTL_DQ58	137	
	BB4	IO_L6N_T0U_N11_AD6N_67_BB4	DDR4_0_RTL_DQ59	282	
	BB9	IO_L2P_T0L_N2_67_BB9	DDR4_0_RTL_DQ60	128	

	BB8	IO_L2N_T0L_N3_67_BB8	DDR4_0_RTL_DQ61	273	
	AW8	IO_L3P_T0L_N4_AD15P_67_AW8	DDR4_0_RTL_DQ62	135	
	AY8	IO_L3N_T0L_N5_AD15N_67_AY8	DDR4_0_RTL_DQ63	280	
	AK22	IO_L24N_T3U_N11_64_AK22	DDR4_0_RTL_DQ64	49	
	AJ22	IO_L24P_T3U_N10_64_AJ22	DDR4_0_RTL_DQ65	194	
	AJ21	IO_L23P_T3U_N8_64_AJ21	DDR4_0_RTL_DQ66	56	
	AJ20	IO_L23N_T3U_N9_64_AJ20	DDR4_0_RTL_DQ67	201	
	AL21	IO_L21N_T3L_N5_AD8N_64_AL21	DDR4_0_RTL_DQ68	47	
	AL22	IO_L21P_T3L_N4_AD8P_64_AL22	DDR4_0_RTL_DQ69	192	
	AM21	IO_L20P_T3L_N2_AD1P_64_AM21	DDR4_0_RTL_DQ70	54	
	AM20	IO_L20N_T3L_N3_AD1N_64_AM20	DDR4_0_RTL_DQ71	199	

Table 19. Signal assignment of PL DIMM0 [J8]


DDR4 DIMM Connector-1
P_12V
DDR4_0_VDDQ
VREF_PL_0_DIMM
DDR4_0_VTT
PL_0_DDR4_SPD_SA2
VCC_2V5
DDR4_0_VREF
DDR4_0_RTL_RESET_N
CN-DDR4-DIMM
CN-DDR4-DIMM


FPGA HP Bank 64 ~ 65
(DDR4_0_DIMM I/F)
BANK 64
BANK 65
XCZU17EG-FFVC1760
DDR4_0_VDDQ
DDR4_0_VREF
VRP_64
VRP_65
R9 47K
R10 240R/1%
R11 240R/1%
R12 100R/1%
C440 100nF
C3 47uF/6.3V/2012
C4 4.7uF
C5 4.7uF
C6 4.7uF
C7 4.7uF
C8 4.7uF
C9 4.7uF
DDR4_0_RTL_ALERT_B
PL_DDR4_0_CLK_300MHZ_P
PL_DDR4_0_CLK_300MHZ_N


FPGA HP Bank 66 ~ 67
(DDR4_0_DIMM & DDR4_1_DIMM I/F)
BANK 66
BANK 67
XCZU7EG-FFVC1760
DDR4_0_VDDQ
DDR4_0_VREF
VRP_66
VRP_67
R13
240R/1%
R247
240R/1%

6.5.2. DIMM1 [J9]

Device	Pin	Pin Name	Schematic Net Name	Pin	Device
U1 (XCZU17EG-FFVC1760)	K24	IO_L4N_T0U_N7_DBC_AD7N_70_K24	DDR4_1_RTL_ODT0	87	J9
	H23	IO_L10P_T1U_N6_QBC_AD4P_70_H23	DDR4_1_RTL_ODT1	91	
	L25	IO_L2N_T0L_N3_70_L25	DDR4_1_RTL_PAR	222	
	A27	IO_L20P_T3L_N2_AD1P_70_A27	DDR4_1_RTL_RESET_N	58	
	B26	IO_L22N_T3U_N7_DBC_AD0N_70_B26	DDR4_1_RTL_ACT_N	62	
	D27	IO_L17P_T2U_N8_AD10P_70_D27	DDR4_1_RTL_ALERT_B	208	
	K25	IO_T1U_N12_70_K25	DDR4_1_RTL_BA0	81	
	H25	IO_L11P_T1U_N8_GC_70_H25	DDR4_1_RTL_BA1	224	
	E26	IO_L16P_T2U_N6_QBC_AD3P_70_E26	DDR4_1_RTL_BG0	63	
	F28	IO_L15N_T2L_N5_AD11N_70_F28	DDR4_1_RTL_BG1	207	
	B27	IO_L21N_T3L_N5_AD8N_70_B27	DDR4_1_RTL_CKE0	60	
	A25	IO_L24N_T3U_N11_70_A25	DDR4_1_RTL_CKE1	203	
	B28	IO_L19N_T3L_N1_DBC_AD9N_70_B28	DDR4_1_RTL_CK_C0	75	
	C28	IO_L19P_T3L_N0_DBC_AD9P_70_C28	DDR4_1_RTL_CK_T0	74	
	A24	IO_L24P_T3U_N10_70_A24	DDR4_1_RTL_CS_N0	84	
	G23	IO_L10N_T1U_N7_QBC_AD4N_70_G23	DDR4_1_RTL_CS_N1	89	
	AJ32	PS_MIO14_AJ32	PS_I2C0_SCL	141	
	AD35	PS_MIO15_AD35	PS_I2C0_SDA	285	
	E24	IO_L18N_T2U_N11_AD2N_70_E24	DDR4_1_RTL_EVENT_B	78	
	F24	IO_L18P_T2U_N10_AD2P_70_F24	DDR4_1_RTL_ADR0	79	
	C24	IO_L23P_T3U_N8_70_C24	DDR4_1_RTL_ADR1	72	
	D24	IO_T3U_N12_70_D24	DDR4_1_RTL_ADR2	216	
	G25	IO_L12N_T1U_N11_GC_70_G25	DDR4_1_RTL_ADR3	71	
	F25	IO_L14P_T2L_N2_GC_70_F25	DDR4_1_RTL_ADR4	214	
	C25	IO_L23N_T3U_N9_70_C25	DDR4_1_RTL_ADR5	213	
	E25	IO_L14N_T2L_N3_GC_70_E25	DDR4_1_RTL_ADR6	69	
	C26	IO_L21P_T3L_N4_AD8P_70_C26	DDR4_1_RTL_ADR7	211	
	B25	IO_L22P_T3U_N6_DBC_AD0P_70_B25	DDR4_1_RTL_ADR8	68	
	A28	IO_L20N_T3L_N3_AD1N_70_A28	DDR4_1_RTL_ADR9	66	
	L24	IO_L4P_T0U_N6_DBC_AD7P_70_L24	DDR4_1_RTL_ADR10	225	
	D26	IO_T2U_N12_70_D26	DDR4_1_RTL_ADR11	210	
	D28	IO_L17N_T2U_N9_AD10N_70_D28	DDR4_1_RTL_ADR12	65	

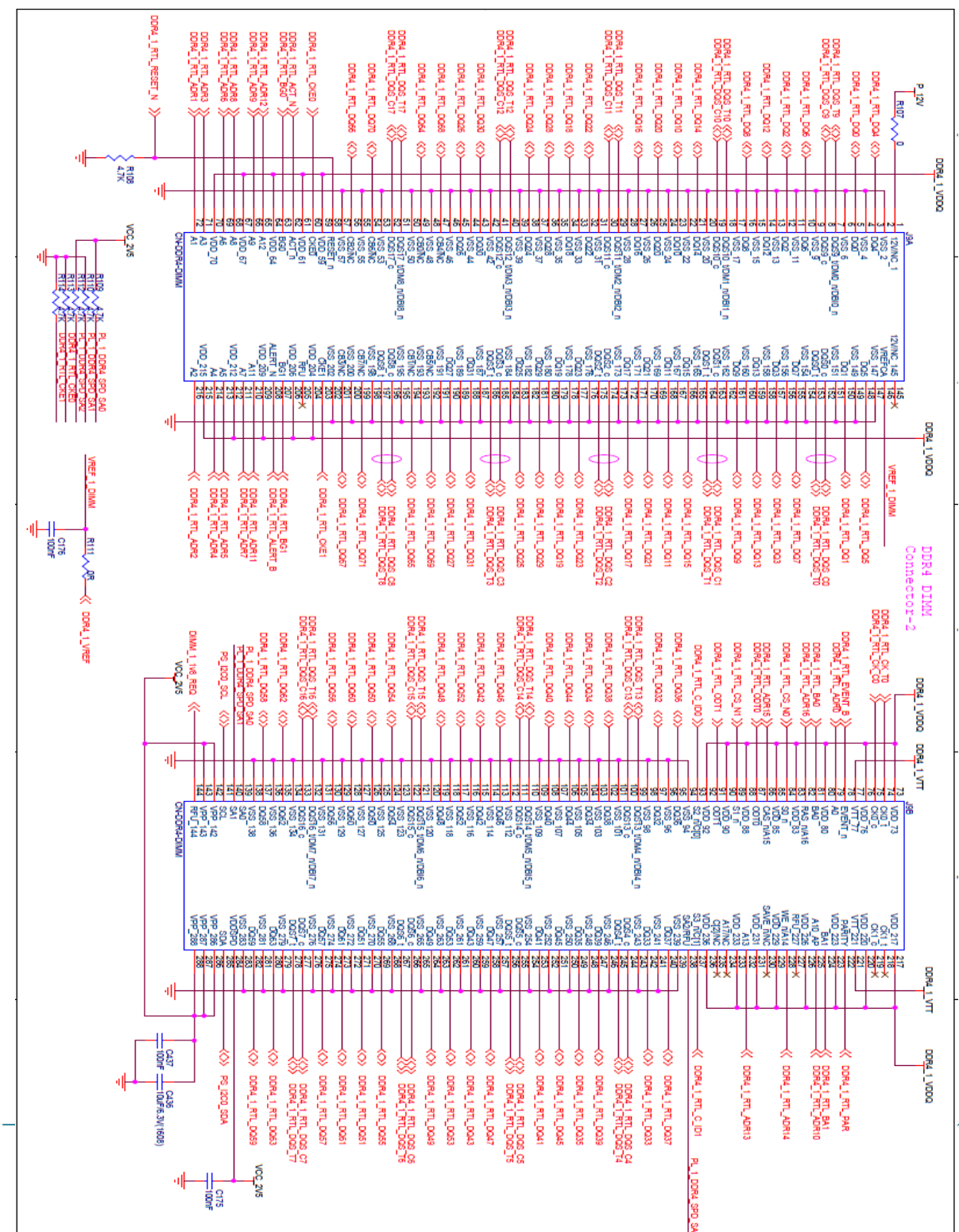
	J23	IO_L9P_T1L_N4_AD12P_70_J23	DDR4_1_RTL_ADR13	232	
	J24	IO_L9N_T1L_N5_AD12N_70_J24	DDR4_1_RTL_ADR14	228	
	H24	IO_L12P_T1U_N10_GC_70_H24	DDR4_1_RTL_ADR15	86	
	H26	IO_L11N_T1U_N9_GC_70_H26	DDR4_1_RTL_ADR16	82	
	C36	IO_L19P_T3L_N0_DBC_AD9P_69_C36	DDR4_1_RTL_DQS_T0	153	
	C37	IO_L19N_T3L_N1_DBC_AD9N_69_C37	DDR4_1_RTL_DQS_C0	152	
	E32	IO_L13P_T2L_N0_GC_QBC_69_E32	DDR4_1_RTL_DQS_T1	164	
	D32	IO_L13N_T2L_N1_GC_QBC_69_D32	DDR4_1_RTL_DQS_C1	163	
	E29	IO_L7P_T1L_N0_QBC_AD13P_69_E29	DDR4_1_RTL_DQS_T2	175	
	D29	IO_L7N_T1L_N1_QBC_AD13N_69_D29	DDR4_1_RTL_DQS_C2	174	
	K29	IO_L1P_T0L_N0_DBC_69_K29	DDR4_1_RTL_DQS_T3	186	
	J29	IO_L1N_T0L_N1_DBC_69_J29	DDR4_1_RTL_DQS_C3	185	
	G22	IO_L13P_T2L_N0_GC_QBC_71_G22	DDR4_1_RTL_DQS_T4	245	
	G21	IO_L13N_T2L_N1_GC_QBC_71_G21	DDR4_1_RTL_DQS_C4	244	
	E16	IO_L19P_T3L_N0_DBC_AD9P_68_E16	DDR4_1_RTL_DQS_T5	256	
	D16	IO_L19N_T3L_N1_DBC_AD9N_68_D16	DDR4_1_RTL_DQS_C5	255	
	H15	IO_L7P_T1L_N0_QBC_AD13P_68_H15	DDR4_1_RTL_DQS_T6	267	
	G15	IO_L7N_T1L_N1_QBC_AD13N_68_G15	DDR4_1_RTL_DQS_C6	266	
	F14	IO_L13P_T2L_N0_GC_QBC_68_F14	DDR4_1_RTL_DQS_T7	278	
	E14	IO_L13N_T2L_N1_GC_QBC_68_E14	DDR4_1_RTL_DQS_C7	277	
	D19	IO_L19P_T3L_N0_DBC_AD9P_71_D19	DDR4_1_RTL_DQS_T8	197	
	C19	IO_L19N_T3L_N1_DBC_AD9N_71_C19	DDR4_1_RTL_DQS_C8	196	
	A39	IO_L22P_T3U_N6_DBC_AD0P_69_A39	DDR4_1_RTL_DQS_T9	7	
	A40	IO_L22N_T3U_N7_DBC_AD0N_69_A40	DDR4_1_RTL_DQS_C9	8	
	D34	IO_L16P_T2U_N6_QBC_AD3P_69_D34	DDR4_1_RTL_DQS_T10	18	
	C34	IO_L16N_T2U_N7_QBC_AD3N_69_C34	DDR4_1_RTL_DQS_C10	19	
	B31	IO_L10P_T1U_N6_QBC_AD4P_69_B31	DDR4_1_RTL_DQS_T11	29	
	A32	IO_L10N_T1U_N7_QBC_AD4N_69_A32	DDR4_1_RTL_DQS_C11	30	
	G30	IO_L4P_T0U_N6_DBC_AD7P_69_G30	DDR4_1_RTL_DQS_T12	40	
	F30	IO_L4N_T0U_N7_DBC_AD7N_69_F30	DDR4_1_RTL_DQS_C12	41	
	F20	IO_L16P_T2U_N6_QBC_AD3P_71_F20	DDR4_1_RTL_DQS_T13	99	
	E20	IO_L16N_T2U_N7_QBC_AD3N_71_E20	DDR4_1_RTL_DQS_C13	100	
	B17	IO_L22P_T3U_N6_DBC_AD0P_68_B17	DDR4_1_RTL_DQS_T14	110	
	A17	IO_L22N_T3U_N7_DBC_AD0N_68_A17	DDR4_1_RTL_DQS_C14	111	

	G18	IO_L10P_T1U_N6_QBC_AD4P_68_G18	DDR4_1_RTL_DQS_T15	121	
	F18	IO_L10N_T1U_N7_QBC_AD4N_68_F18	DDR4_1_RTL_DQS_C15	122	
	B13	IO_L16P_T2U_N6_QBC_AD3P_68_B13	DDR4_1_RTL_DQS_T16	132	
	A12	IO_L16N_T2U_N7_QBC_AD3N_68_A12	DDR4_1_RTL_DQS_C16	133	
	B21	IO_L22N_T3U_N7_DBC_AD0N_71_B21	DDR4_1_RTL_DQS_T17	51	
	C21	IO_L22P_T3U_N6_DBC_AD0P_71_C21	DDR4_1_RTL_DQS_C17	52	
	B37	IO_L20N_T3L_N3_AD1N_69_B37	DDR4_1_RTL_DQ0	5	
	A38	IO_L21N_T3L_N5_AD8N_69_A38	DDR4_1_RTL_DQ1	150	
	A37	IO_L21P_T3L_N4_AD8P_69_A37	DDR4_1_RTL_DQ2	12	
	B36	IO_L20P_T3L_N2_AD1P_69_B36	DDR4_1_RTL_DQ3	157	
	B42	IO_L24N_T3U_N11_69_B42	DDR4_1_RTL_DQ4	3	
	C42	IO_L24P_T3U_N10_69_C42	DDR4_1_RTL_DQ5	148	
	B41	IO_L23N_T3U_N9_69_B41	DDR4_1_RTL_DQ6	10	
	B40	IO_L23P_T3U_N8_69_B40	DDR4_1_RTL_DQ7	155	
	C33	IO_L15N_T2L_N5_AD11N_69_C33	DDR4_1_RTL_DQ8	16	
	D33	IO_L15P_T2L_N4_AD11P_69_D33	DDR4_1_RTL_DQ9	161	
	B33	IO_L14N_T2L_N3_GC_69_B33	DDR4_1_RTL_DQ10	23	
	B32	IO_L14P_T2L_N2_GC_69_B32	DDR4_1_RTL_DQ11	168	
	B35	IO_L17P_T2U_N8_AD10P_69_B35	DDR4_1_RTL_DQ12	14	
	A35	IO_L17N_T2U_N9_AD10N_69_A35	DDR4_1_RTL_DQ13	159	
	A34	IO_L18N_T2U_N11_AD2N_69_A34	DDR4_1_RTL_DQ14	21	
	A33	IO_L18P_T2U_N10_AD2P_69_A33	DDR4_1_RTL_DQ15	166	
	B30	IO_L8N_T1L_N3_AD5N_69_B30	DDR4_1_RTL_DQ16	27	
	A30	IO_L9N_T1L_N5_AD12N_69_A30	DDR4_1_RTL_DQ17	172	
	C29	IO_L8P_T1L_N2_AD5P_69_C29	DDR4_1_RTL_DQ18	34	
	A29	IO_L9P_T1L_N4_AD12P_69_A29	DDR4_1_RTL_DQ19	179	
	D31	IO_L11N_T1U_N9_GC_69_D31	DDR4_1_RTL_DQ20	25	
	E31	IO_L11P_T1U_N8_GC_69_E31	DDR4_1_RTL_DQ21	170	
	C30	IO_L12P_T1U_N10_GC_69_C30	DDR4_1_RTL_DQ22	32	
	C31	IO_L12N_T1U_N11_GC_69_C31	DDR4_1_RTL_DQ23	177	
	F31	IO_L3P_T0L_N4_AD15P_69_F31	DDR4_1_RTL_DQ24	38	
	F32	IO_L3N_T0L_N5_AD15N_69_F32	DDR4_1_RTL_DQ25	183	
	J30	IO_L2P_T0L_N2_69_J30	DDR4_1_RTL_DQ26	45	
	H30	IO_L2N_T0L_N3_69_H30	DDR4_1_RTL_DQ27	190	

	G28	IO_L5P_T0U_N8_AD14P_69_G28	DDR4_1_RTL_DQ28	36	
	F29	IO_L5N_T0U_N9_AD14N_69_F29	DDR4_1_RTL_DQ29	181	
	J28	IO_L6P_T0U_N10_AD6P_69_J28	DDR4_1_RTL_DQ30	43	
	H28	IO_L6N_T0U_N11_AD6N_69_H28	DDR4_1_RTL_DQ31	188	
	F23	IO_L14P_T2L_N2_GC_71_F23	DDR4_1_RTL_DQ32	97	
	F22	IO_L14N_T2L_N3_GC_71_F22	DDR4_1_RTL_DQ33	242	
	F19	IO_L15P_T2L_N4_AD11P_71_F19	DDR4_1_RTL_DQ34	104	
	E19	IO_L15N_T2L_N5_AD11N_71_E19	DDR4_1_RTL_DQ35	249	
	D22	IO_L18N_T2U_N11_AD2N_71_D22	DDR4_1_RTL_DQ36	95	
	E22	IO_L18P_T2U_N10_AD2P_71_E22	DDR4_1_RTL_DQ37	240	
	D21	IO_L17N_T2U_N9_AD10N_71_D21	DDR4_1_RTL_DQ38	102	
	E21	IO_L17P_T2U_N8_AD10P_71_E21	DDR4_1_RTL_DQ39	247	
	D17	IO_L21N_T3L_N5_AD8N_68_D17	DDR4_1_RTL_DQ40	108	
	E17	IO_L21P_T3L_N4_AD8P_68_E17	DDR4_1_RTL_DQ41	253	
	B16	IO_L20N_T3L_N3_AD1N_68_B16	DDR4_1_RTL_DQ42	115	
	C16	IO_L20P_T3L_N2_AD1P_68_C16	DDR4_1_RTL_DQ43	260	
	A18	IO_L24N_T3U_N11_68_A18	DDR4_1_RTL_DQ44	106	
	B18	IO_L24P_T3U_N10_68_B18	DDR4_1_RTL_DQ45	251	
	C18	IO_L23N_T3U_N9_68_C18	DDR4_1_RTL_DQ46	113	
	D18	IO_L23P_T3U_N8_68_D18	DDR4_1_RTL_DQ47	258	
	H18	IO_L9N_T1L_N5_AD12N_68_H18	DDR4_1_RTL_DQ48	119	
	J18	IO_L9P_T1L_N4_AD12P_68_J18	DDR4_1_RTL_DQ49	264	
	H16	IO_L8N_T1L_N3_AD5N_68_H16	DDR4_1_RTL_DQ50	126	
	J16	IO_L8P_T1L_N2_AD5P_68_J16	DDR4_1_RTL_DQ51	271	
	G17	IO_L11P_T1U_N8_GC_68_G17	DDR4_1_RTL_DQ52	117	
	F17	IO_L11N_T1U_N9_GC_68_F17	DDR4_1_RTL_DQ53	262	
	G16	IO_L12P_T1U_N10_GC_68_G16	DDR4_1_RTL_DQ54	124	
	F15	IO_L12N_T1U_N11_GC_68_F15	DDR4_1_RTL_DQ55	269	
	E15	IO_L14P_T2L_N2_GC_68_E15	DDR4_1_RTL_DQ56	130	
	D14	IO_L14N_T2L_N3_GC_68_D14	DDR4_1_RTL_DQ57	275	
	C13	IO_L15N_T2L_N5_AD11N_68_C13	DDR4_1_RTL_DQ58	137	
	D13	IO_L15P_T2L_N4_AD11P_68_D13	DDR4_1_RTL_DQ59	282	
	B15	IO_L18N_T2U_N11_AD2N_68_B15	DDR4_1_RTL_DQ60	128	
	C15	IO_L18P_T2U_N10_AD2P_68_C15	DDR4_1_RTL_DQ61	273	

	A14	IO_L17P_T2U_N8_AD10P_68_A14	DDR4_1_RTL_DQ62	135	
	A13	IO_L17N_T2U_N9_AD10N_68_A13	DDR4_1_RTL_DQ63	280	
	A20	IO_L21P_T3L_N4_AD8P_71_A20	DDR4_1_RTL_DQ64	49	
	B20	IO_L20N_T3L_N3_AD1N_71_B20	DDR4_1_RTL_DQ65	194	
	A19	IO_L21N_T3L_N5_AD8N_71_A19	DDR4_1_RTL_DQ66	56	
	C20	IO_L20P_T3L_N2_AD1P_71_C20	DDR4_1_RTL_DQ67	201	
	A23	IO_L24N_T3U_N11_71_A23	DDR4_1_RTL_DQ68	47	
	B23	IO_L24P_T3U_N10_71_B23	DDR4_1_RTL_DQ69	192	
	B22	IO_L23P_T3U_N8_71_B22	DDR4_1_RTL_DQ70	54	
	A22	IO_L23N_T3U_N9_71_A22	DDR4_1_RTL_DQ71	199	

Table 20. Signal assignment of PL DIMM1 [J9]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J9A
J9B
CN-DDR4-DIMM
R107
R108
R111
C176
C437
C436
C175
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DDR4_1_RTL_ACT_N
DDR4_1_RTL_ALERT_B
DDR4_1_RTL_PAR
DDR4_1_RTL_EVENT_B
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DDR4_1_RTL_CS_N0
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PU_1_DDR4_C_D0
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PD_1_DDR4_ALERT_B
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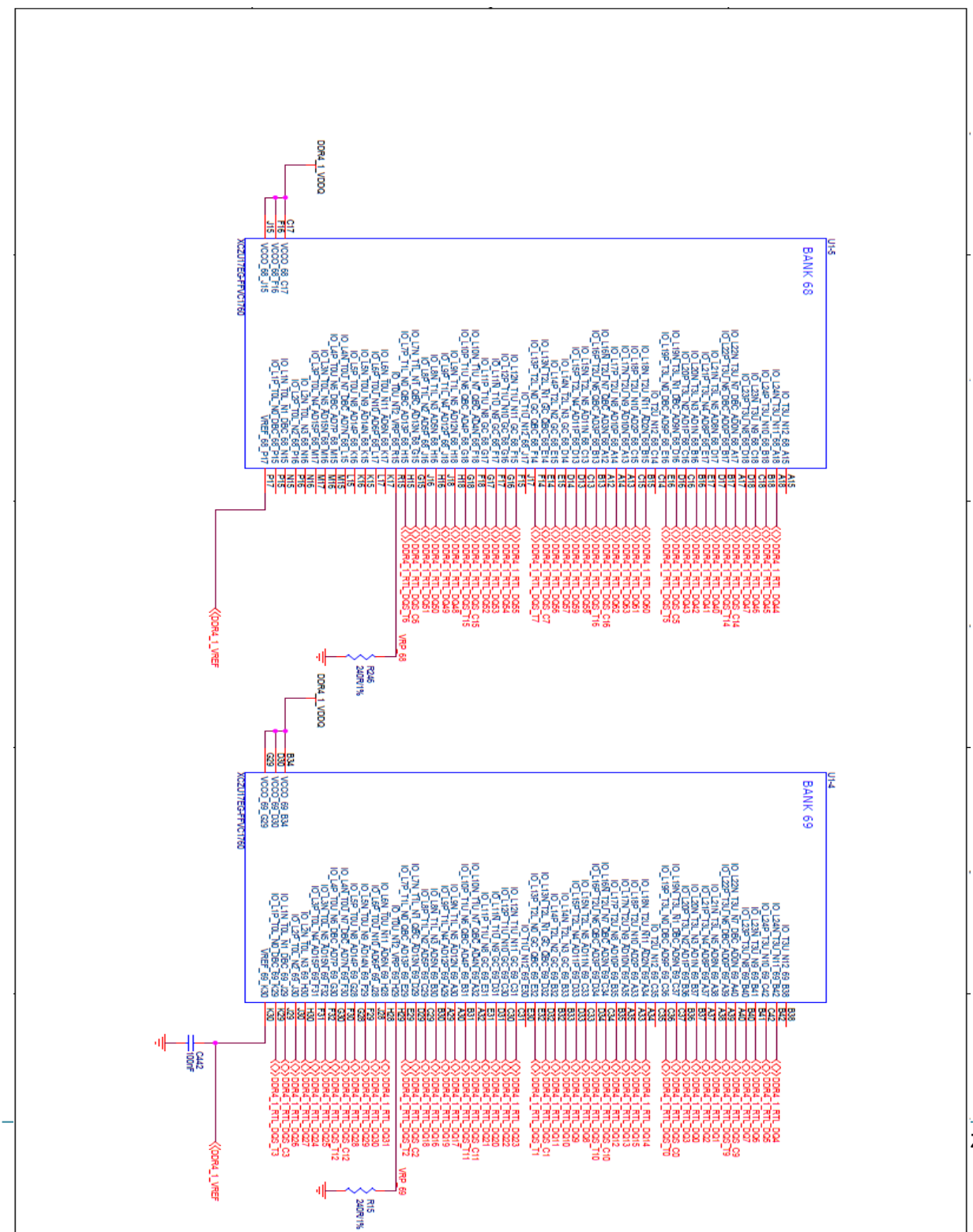
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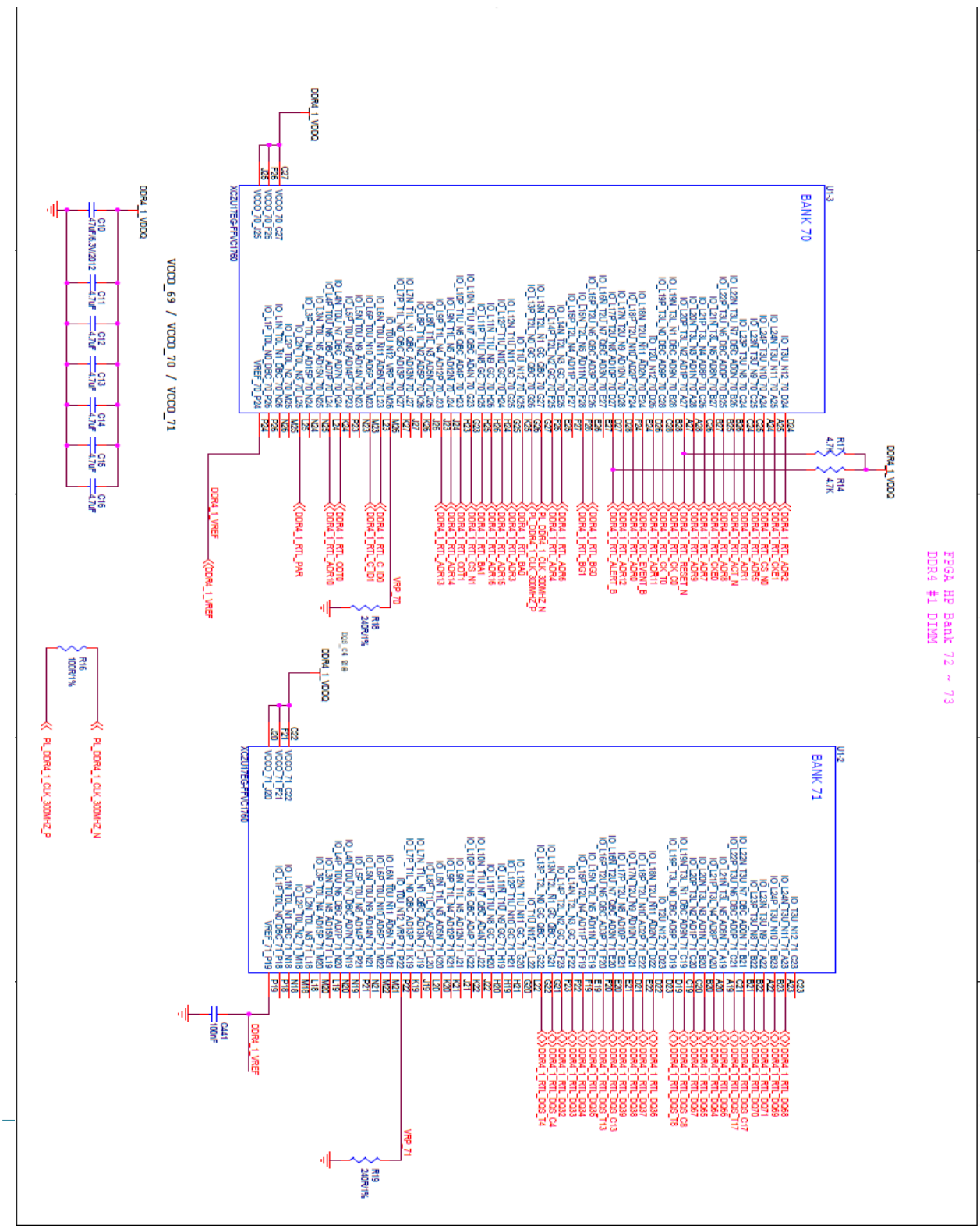
R15
240R/1%
C442
100nF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VCCO_69 / VCCO_70 / VCCO_71
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BANK 71
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DDR4_1_VREF
VRP_70
VRP_71
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PL_DDR4_1_CLK_300MHZ_P

6.6. PCIe x16 Endpoint [J11]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	D9	IO_L12P_AD0P_93_D9	PCIE_PERST_B_CON	PERST#	A11	J11
	L27	PS_MIO26_L27	PCIE_WAKE_B_CON	WAKE#	B11	
	AH11	MGTREFCLK0N_225_AH11	PCIE_REFCLK_N	REFCLKn	A14	
	AH12	MGTREFCLK0P_225_AH12	PCIE_REFCLK_P	REFCLKp	A13	
	AK11	MGTREFCLK0N_224_AK11	B224_REFCLK_N	OUT0b	23	U8
	AK12	MGTREFCLK0P_224_AK12	B224_REFCLK_P	OUT0	24	
	AG9	MGTREFCLK1N_225_AG9	B225_REFCLK_N	OUT0Ab	20	
	AG10	MGTREFCLK1P_225_AG10	B225_REFCLK_P	OUT0A	21	
	AF11	MGTREFCLK0N_226_AF11	B226_REFCLK_N	OUT1b	27	
	AF12	MGTREFCLK0P_226_AF12	B226_REFCLK_P	OUT1	28	
	AD11	MGTREFCLK0N_227_AD11	B227_REFCLK_N	OUT2b	30	
	AD12	MGTREFCLK0P_227_AD12	B227_REFCLK_P	OUT2	31	
	AD7	MGTHTXN3_227_AD7	PCIE_TX0_N	PETn0	B15	J11
	AD8	MGTHTXP3_227_AD8	PCIE_TX0_P	PETp0	B14	
	AE5	MGTHTXN2_227_AE5	PCIE_TX1_N	PETn1	B20	
	AE6	MGTHTXP2_227_AE6	PCIE_TX1_P	PETp1	B19	
	AF7	MGTHTXN1_227_AF7	PCIE_TX2_N	PETn2	B24	
	AF8	MGTHTXP1_227_AF8	PCIE_TX2_P	PETp2	B23	
	AG5	MGTHTXN0_227_AG5	PCIE_TX3_N	PETn3	B28	
	AG6	MGTHTXP0_227_AG6	PCIE_TX3_P	PETp3	B27	
	AH7	MGTHTXN3_226_AH7	PCIE_TX4_N	PETn4	B34	
	AH8	MGTHTXP3_226_AH8	PCIE_TX4_P	PETp4	B33	
	AJ5	MGTHTXN2_226_AJ5	PCIE_TX5_N	PETn5	B38	
	AJ6	MGTHTXP2_226_AJ6	PCIE_TX5_P	PETp5	B37	
	AK7	MGTHTXN1_226_AK7	PCIE_TX6_N	PETn6	B42	
	AK8	MGTHTXP1_226_AK8	PCIE_TX6_P	PETp6	B41	
	AL5	MGTHTXN0_226_AL5	PCIE_TX7_P	PETn7	B46	
	AL6	MGTHTXP0_226_AL6	PCIE_TX7_N	PETp7	B45	
	AM7	MGTHTXN3_225_AM7	PCIE_TX8_N	PETn8	B51	
	AM8	MGTHTXP3_225_AM8	PCIE_TX8_P	PETp8	B50	
	AN5	MGTHTXN2_225_AN5	PCIE_TX9_N	PETn9	B55	

	AN6	MGTHTXP2_225_AN6	PCIE_TX9_P	PETp9	B54	
	AP7	MGTHTXN1_225_AP7	PCIE_TX10_N	PETn10	B59	
	AP8	MGTHTXP1_225_AP8	PCIE_TX10_P	PETp10	B58	
	AR5	MGTHTXN0_225_AR5	PCIE_TX11_N	PETn11	B63	
	AR6	MGTHTXP0_225_AR6	PCIE_TX11_P	PETp11	B62	
	AT7	MGTHTXN3_224_AT7	PCIE_TX12_N	PETn12	B67	
	AT8	MGTHTXP3_224_AT8	PCIE_TX12_P	PETp12	B66	
	AU5	MGTHTXN2_224_AU5	PCIE_TX13_N	PETn13	B71	
	AU6	MGTHTXP2_224_AU6	PCIE_TX13_P	PETp13	B70	
	AW5	MGTHTXN1_224_AW5	PCIE_TX14_N	PETn14	B75	
	AW6	MGTHTXP1_224_AW6	PCIE_TX14_P	PETp14	B74	
	AY3	MGTHTXN0_224_AY3	PCIE_TX15_N	PETn15	B79	
	AY4	MGTHTXP0_224_AY4	PCIE_TX15_P	PETp15	B78	
	AH3	MGTHRXN0_227_AH3	PCIE_RX0_P	PERp0	A16	
	AG1	MGTHRXN1_227_AG1	PCIE_RX0_N	PERn0	A17	
	AE2	MGTHRXP3_227_AE2	PCIE_RX1_P	PERp1	A21	
	AE1	MGTHRXN3_227_AE1	PCIE_RX1_N	PERn1	A22	
	AG2	MGTHRXP1_227_AG2	PCIE_RX2_P	PERp2	A25	
	AG1	MGTHRXN1_227_AG1	PCIE_RX2_N	PERn2	A26	
	AH4	MGTHRXP0_227_AH4	PCIE_RX3_P	PERp3	A29	
	AH3	MGTHRXN0_227_AH3	PCIE_RX3_N	PERn3	A30	
	AJ2	MGTHRXP3_226_AJ2	PCIE_RX4_P	PERp4	A35	
	AJ1	MGTHRXN3_226_AJ1	PCIE_RX4_N	PERn4	A36	
	AK4	MGTHRXP2_226_AK4	PCIE_RX5_P	PERp5	A39	
	AK3	MGTHRXN2_226_AK3	PCIE_RX5_N	PERn5	A40	
	AL2	MGTHRXP1_226_AL2	PCIE_RX6_P	PERp6	A43	
	AL1	MGTHRXN1_226_AL1	PCIE_RX6_N	PERn6	A44	
	AM4	MGTHRXP0_226_AM4	PCIE_RX7_P	PERp7	A47	
	AM3	MGTHRXN0_226_AM3	PCIE_RX7_N	PERn7	A48	
	AN2	MGTHRXP3_225_AN2	PCIE_RX8_P	PERp8	A52	
	AN1	MGTHRXN3_225_AN1	PCIE_RX8_N	PERn8	A53	
	AP4	MGTHRXP2_225_AP4	PCIE_RX9_P	PERp9	A56	
	AP3	MGTHRXN2_225_AP3	PCIE_RX9_N	PERn9	A57	
	AR2	MGTHRXP1_225_AR2	PCIE_RX10_P	PERp10	A60	

	AR1	MGTHRXN1_225_AR1	PCIE_RX10_N	PERn10	A61	
	AT4	MGTHRXP0_225_AT4	PCIE_RX11_P	PERp11	A64	
	AT3	MGTHRXN0_225_AT3	PCIE_RX11_N	PERn11	A65	
	AU2	MGTHRXP3_224_AU2	PCIE_RX12_P	PERp12	A68	
	AU1	MGTHRXN3_224_AU1	PCIE_RX12_N	PERn12	A69	
	AV4	MGTHRXP2_224_AV4	PCIE_RX13_P	PERp13	A72	
	AV3	MGTHRXN2_224_AV3	PCIE_RX13_N	PERn13	A73	
	AW2	MGTHRXP1_224_AW2	PCIE_RX14_P	PERp14	A76	
	AW1	MGTHRXN1_224_AW1	PCIE_RX14_N	PERn14	A77	
	BA2	MGTHRXP0_224_BA2	PCIE_RX15_P	PERp15	A80	
	BA1	MGTHRXN0_224_BA1	PCIE_RX15_N	PERn15	A81	

Table 21. Signal assignment of PCIe x16 Endpoint [J11]

6.7. 1G Ethernet PHY[U16]-Ethernet 1G[J10]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U1	N28	PS_MIO33_N28	ENET_RESET_B	RSTn	1	U16
	P27	PS_MIO34_P27	ENET_INT	INT	20	
	AD32	PS_MIO64_AD32	ENET_TX_CLK	GTX_CLK	33	
	AE29	PS_MIO65_AE29	ENET_TXD0	TXD0	34	
	AD33	PS_MIO66_AD33	ENET_TXD1	TXD1	35	
	AE30	PS_MIO67_AE30	ENET_TXD2	TXD2	36	
	AE33	PS_MIO68_AE33	ENET_TXD3	TXD3	37	
	AE32	PS_MIO69_AE32	ENET_TX_EN	TX_EN	32	
	AF30	PS_MIO70_AF30	ENET_RX_CLK	RX_CLK	31	
	AF31	PS_MIO71_AF31	ENET_RXD0	RXD0	29	
	AF32	PS_MIO72_AF32	ENET_RXD1	RXD1	28	
	AG30	PS_MIO73_AG30	ENET_RXD2	RXD2	26	
	AG33	PS_MIO74_AG33	ENET_RXD3	RXD3	25	
	AF33	PS_MIO75_AF33	ENET_RX_DV	RX_DV	30	
	AH31	PS_MIO76_AH31	ENET_MDC	MDC	40	

	AG31	PS_MIO77_AG31	ENET_MDIO	MDIO	39	

Table 22. Signal assignment of Ethernet

6.8. USB to Dual UART[U40] – USB Micro[J26]

Device	Pin	Pin Name	Schematic Net Name	Pin Name	Pin	Device
U123	13	TXD_ECI	USB_UART1_TXD	PS_MIO20_AH34	AH34	U1
	12	RXD_ECI	USB_UART1_RXD	PS_MIO21_AF35	AF35	
	21	TXD_SCI	USB_UART0_TXD	PS_MIO19_AE35	AE35	
	20	RXD_SCI	USB_UART0_RXD	PS_MIO18_AE34	AE34	
	3	D_P	UHUB_DP2	DP	3	J26
	4	D_N	UHUB_DM2	DM	2	

Table 23. Signal assignment of USB [J26] to Dual UART